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CAD Note:

Property: BUILD-OPT
DNP = Do Not Place

DBG_S - Replace with board short for MP
DBG_R - Replace with lower cost component for MP
DBG_N - Install for Non-Debug Builds
DBG_D - Remove from BOM (Depopulate) for MP
DBG_T - Used for Telemetry in MP as needed
DBG_TS - Used for Telemetry in MP as needed. This part needs to be replaced with a short if telemetry is not needed.

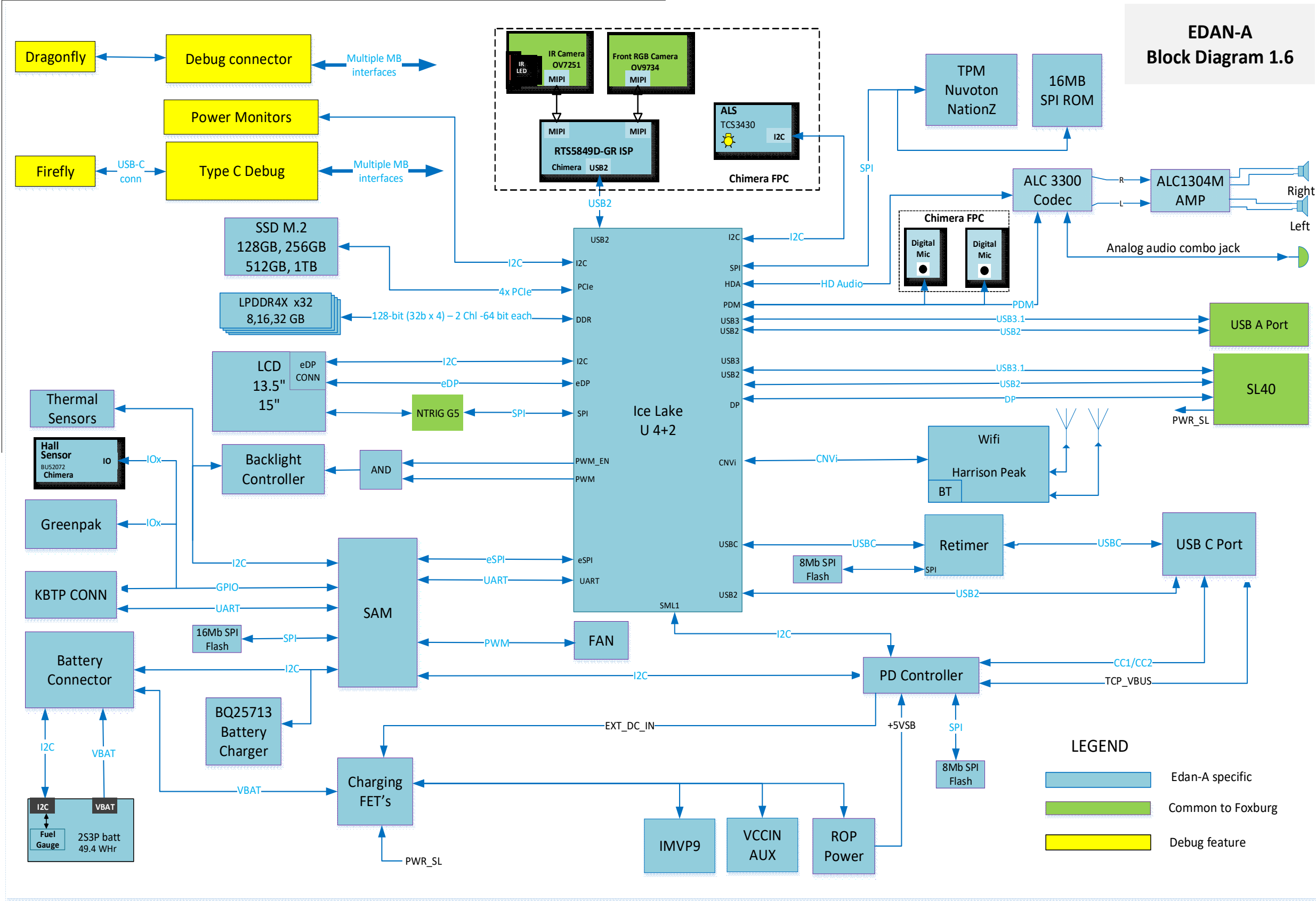
<Variant Name>

Title: Table of Contents		
Engineer: <OrgAddr1>		
Size A3	Project Name EDAN_A_EV1	Rev <RevCode>
Date: Tuesday, May 21, 2019		
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CAD Note:

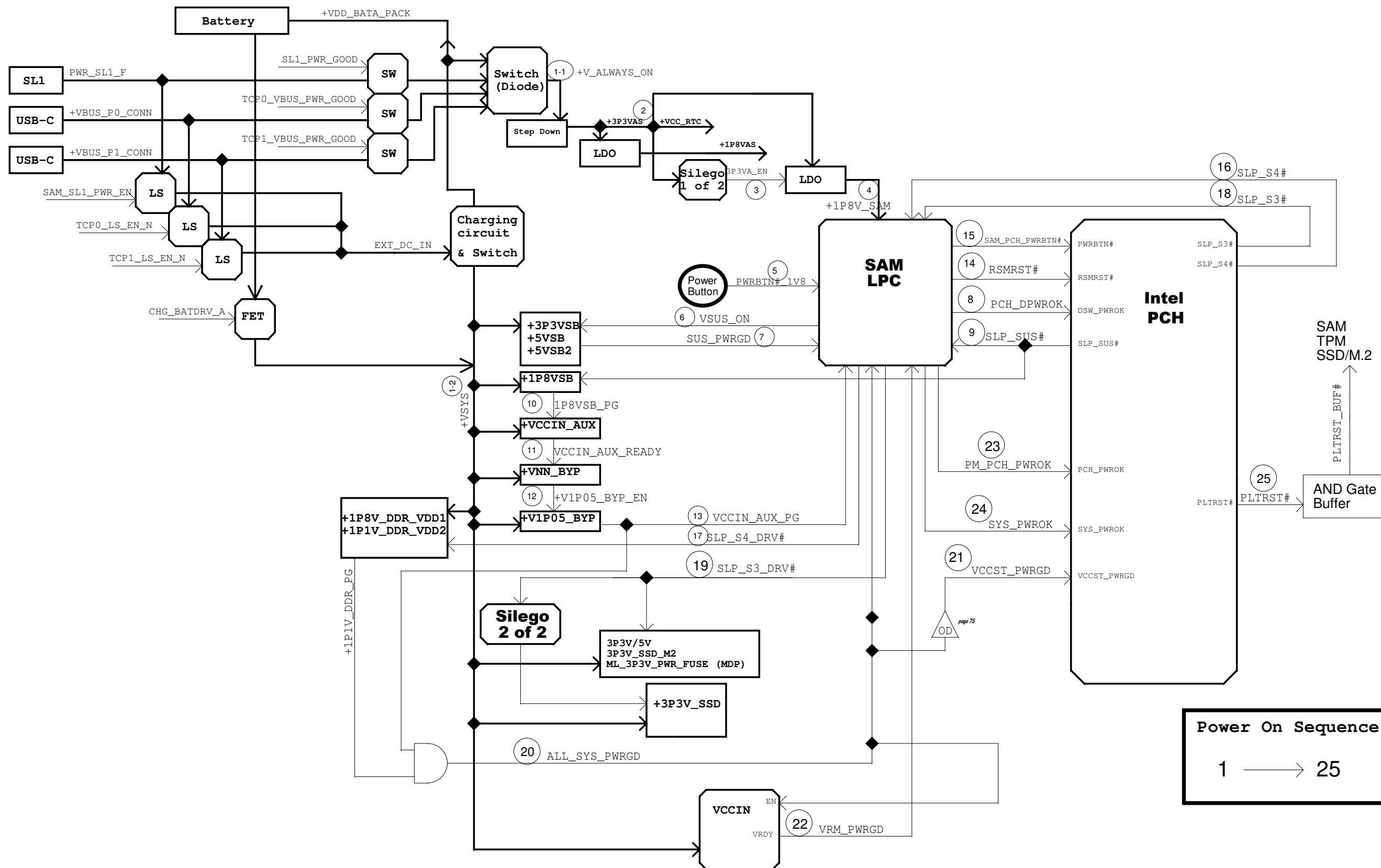
Defaults: Footprint SMD 0201, Cap tmp Coeff X5R, 1% resistors

Title: Build Options		
Engineer: <OrgAddr1>		
Size A3	Project Name EDAN_A_EV1	Rev 1.00
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SIGNAL & RESET MAP

Last Update - Feb 13 2018

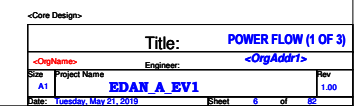


Power On Sequence

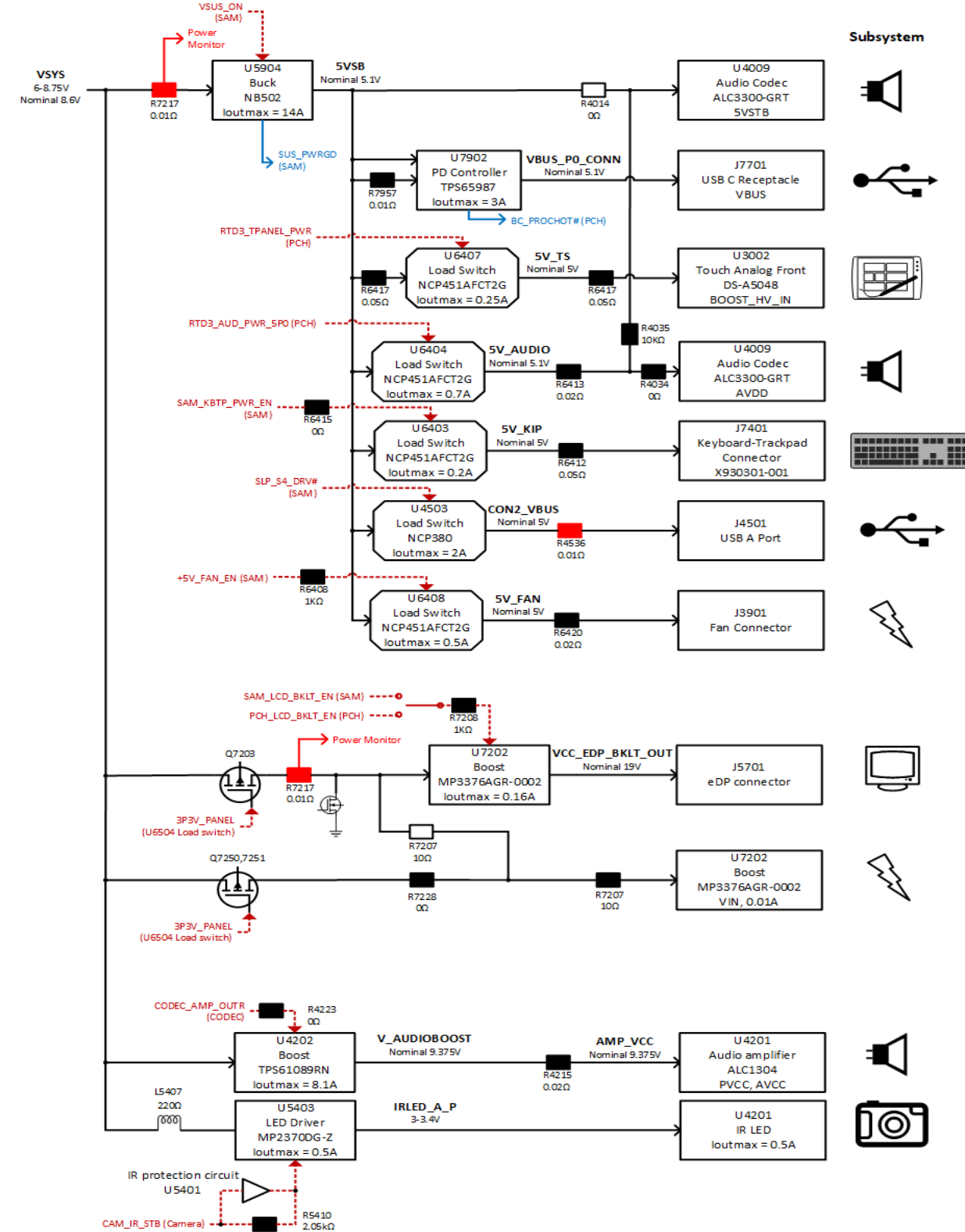
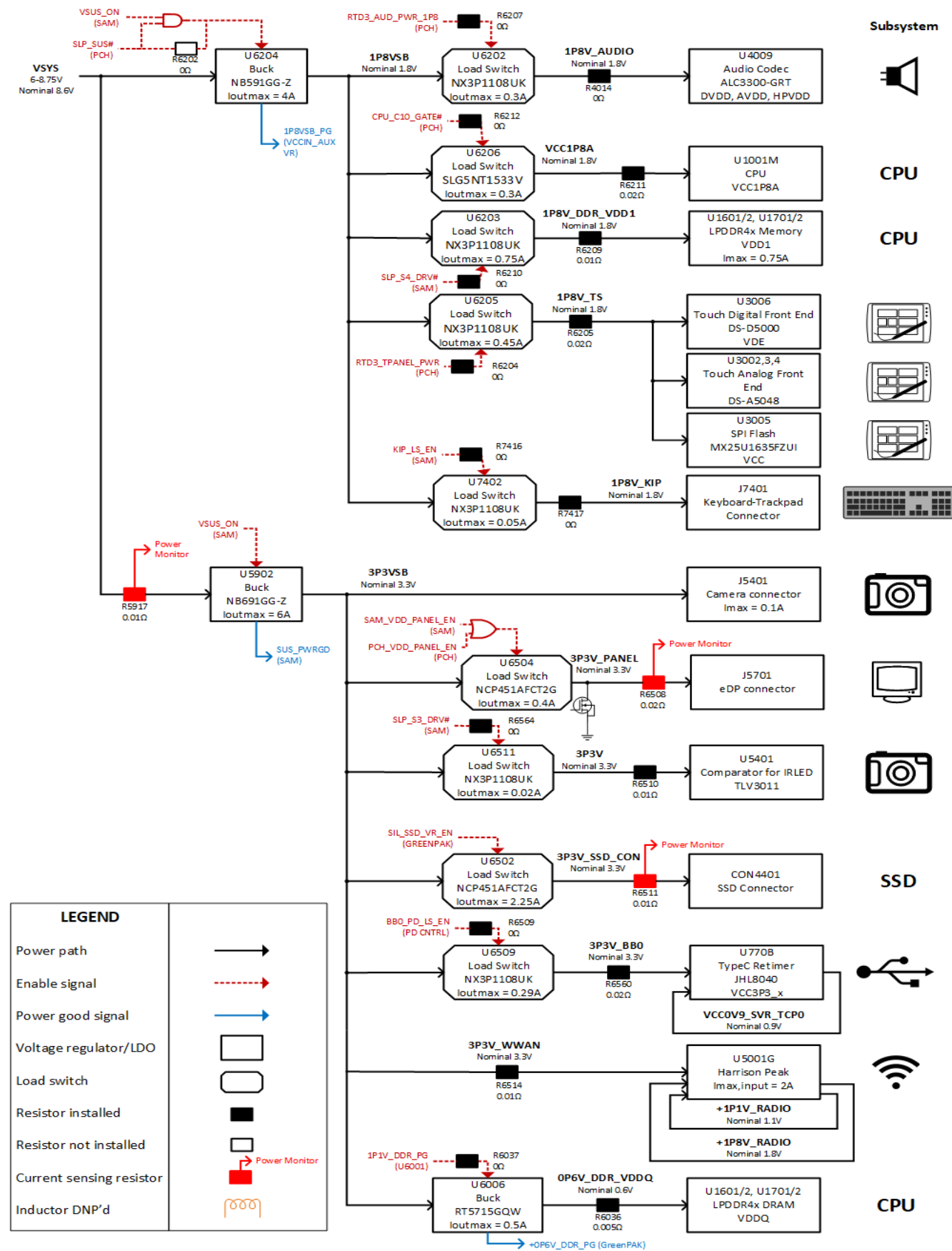
1 \longrightarrow 25

EDAN/HOOK Power Flow EV1

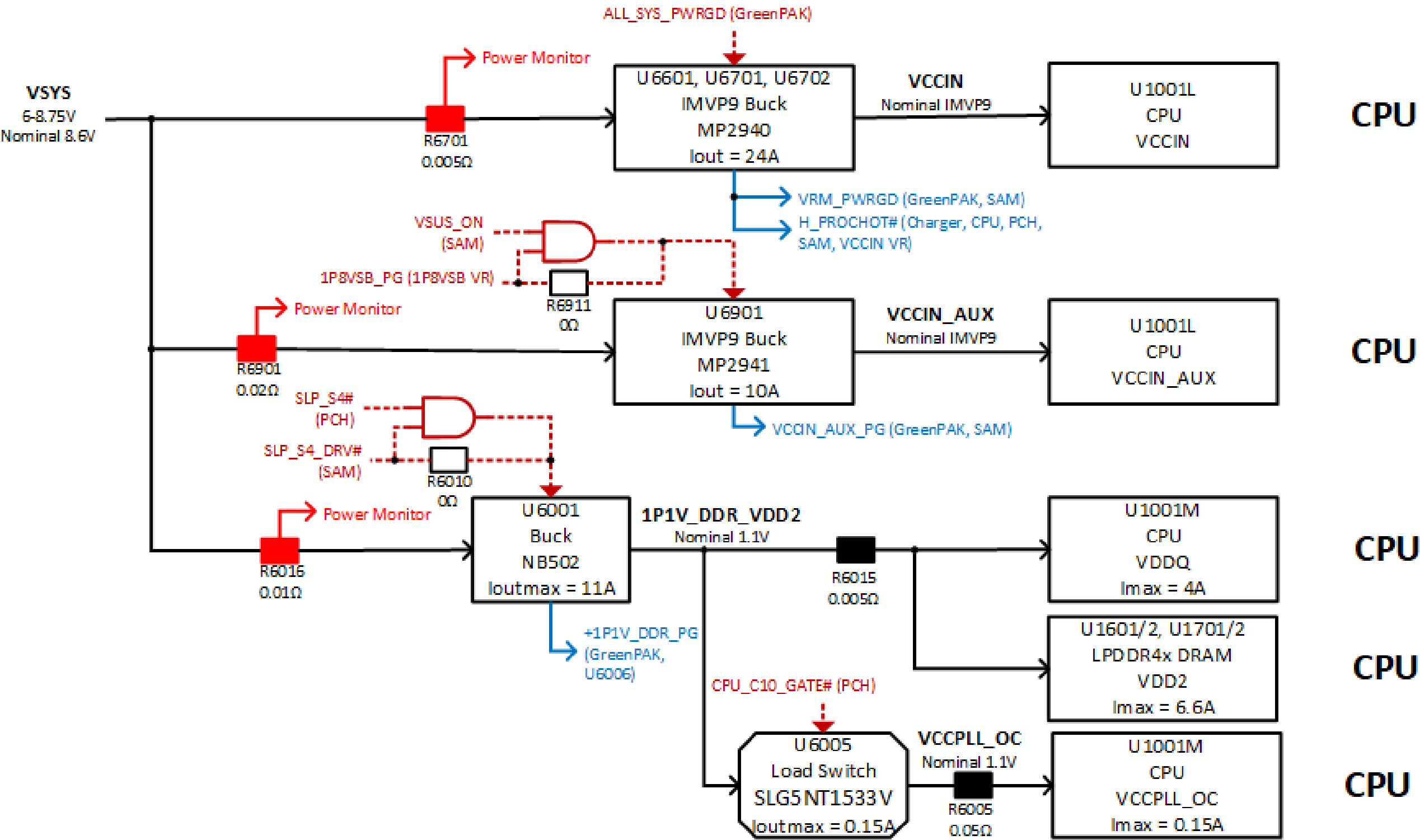
INTERMEDIATE BUSES

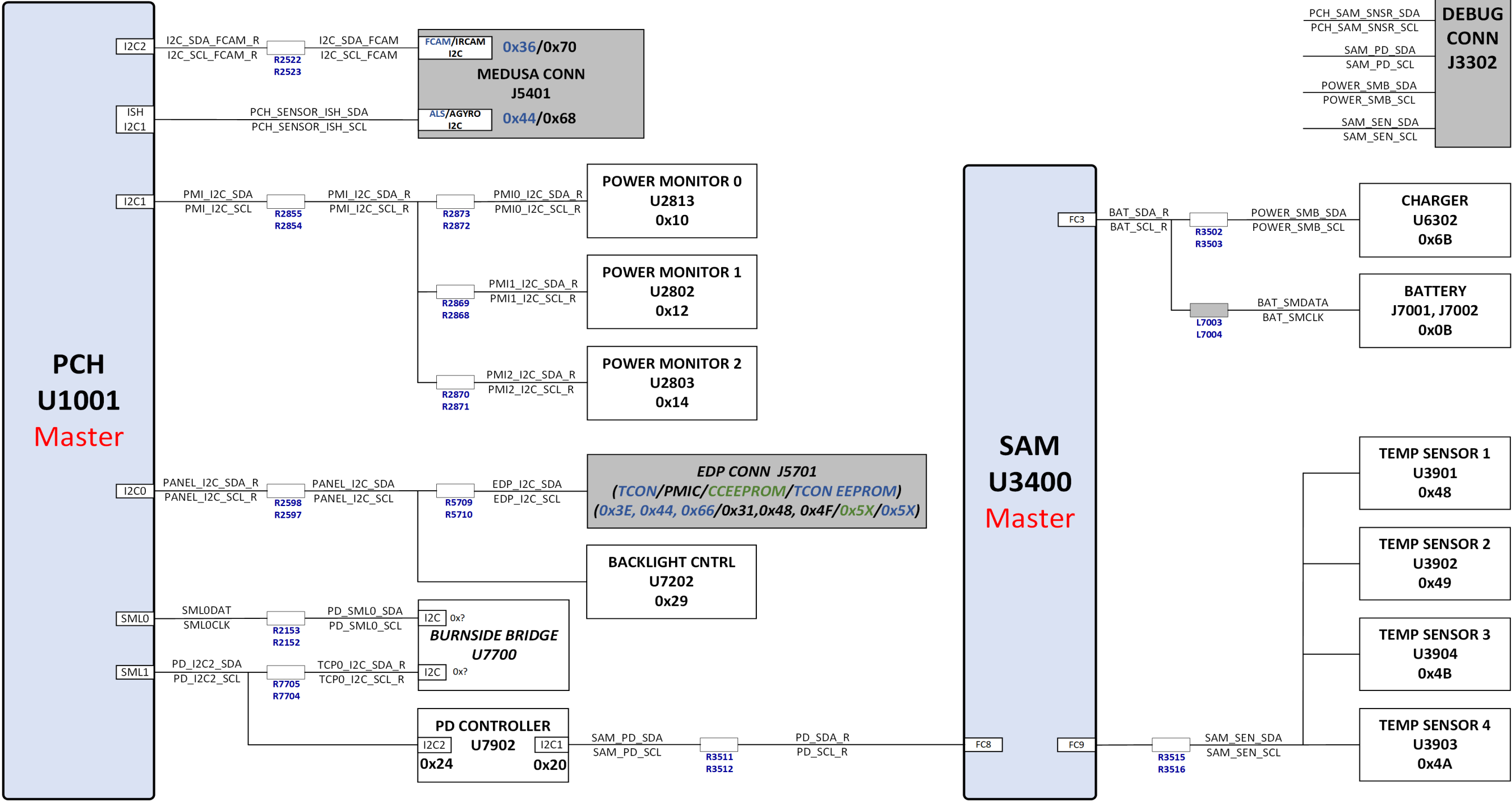


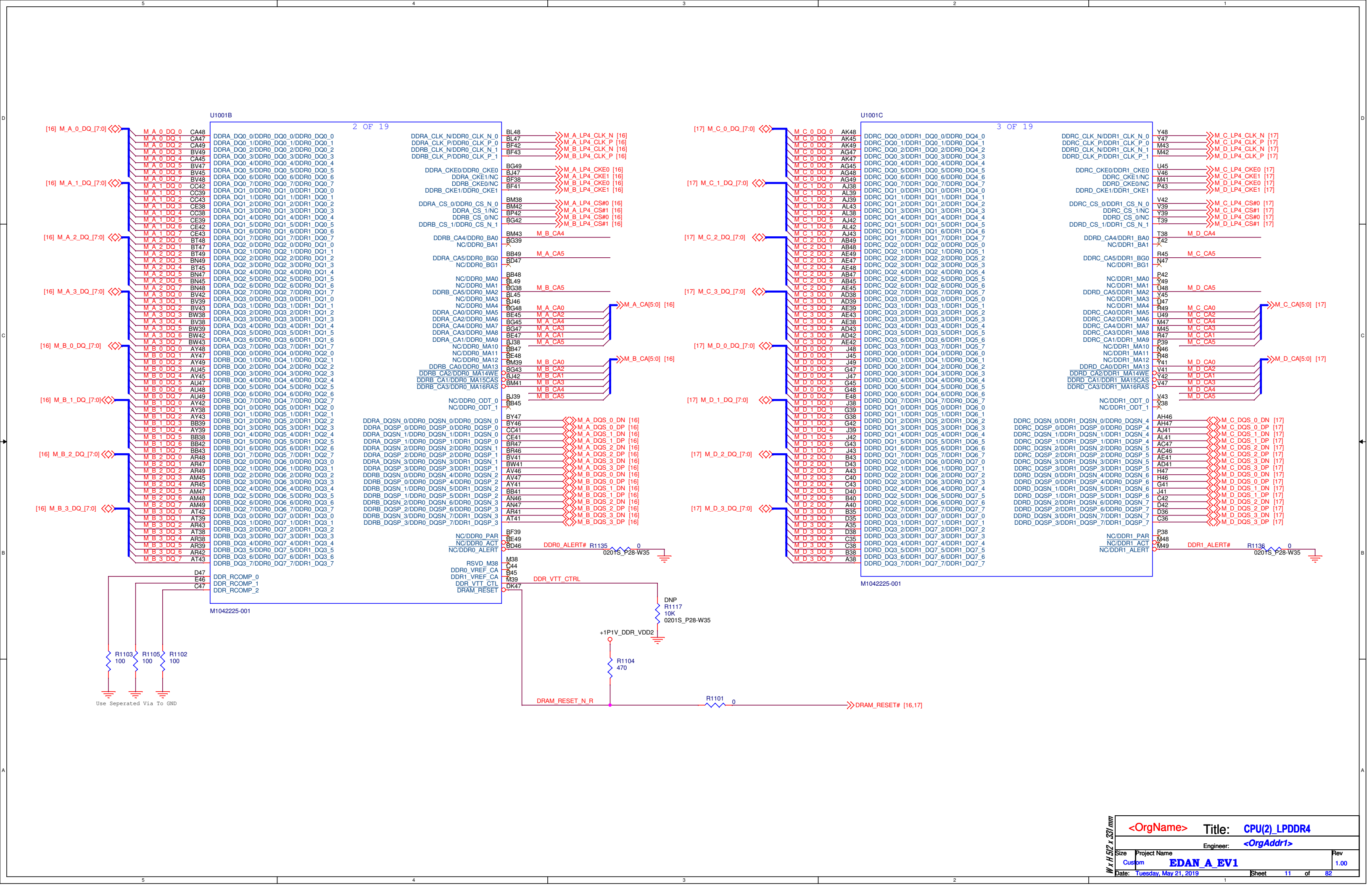
POINT OF LOAD REGULATORS AND LOAD SWITCHES

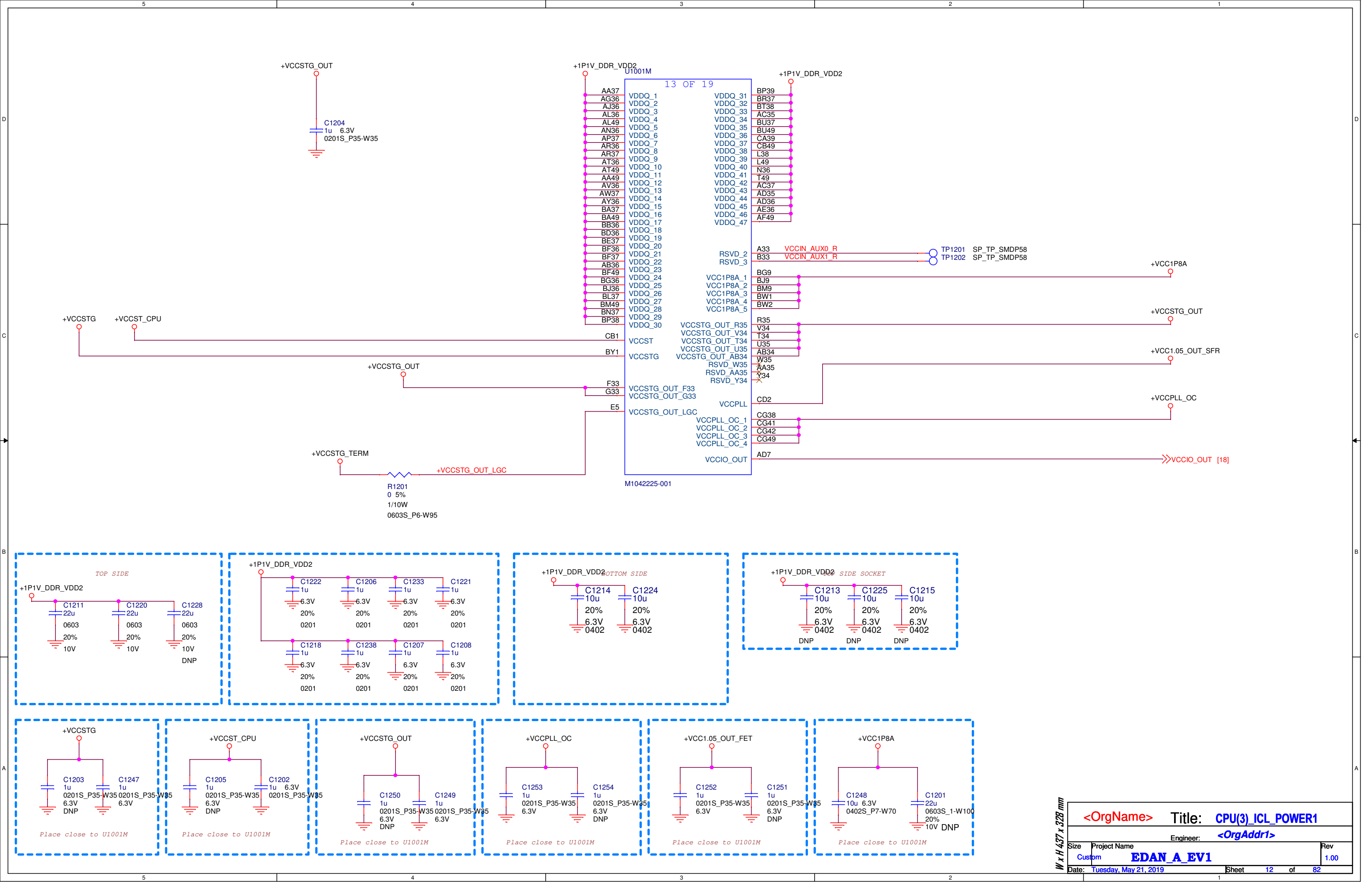


CPU Power Delivery











W x H 347 x 225 mm

<OrgName>

Title: CPU(5)_GND

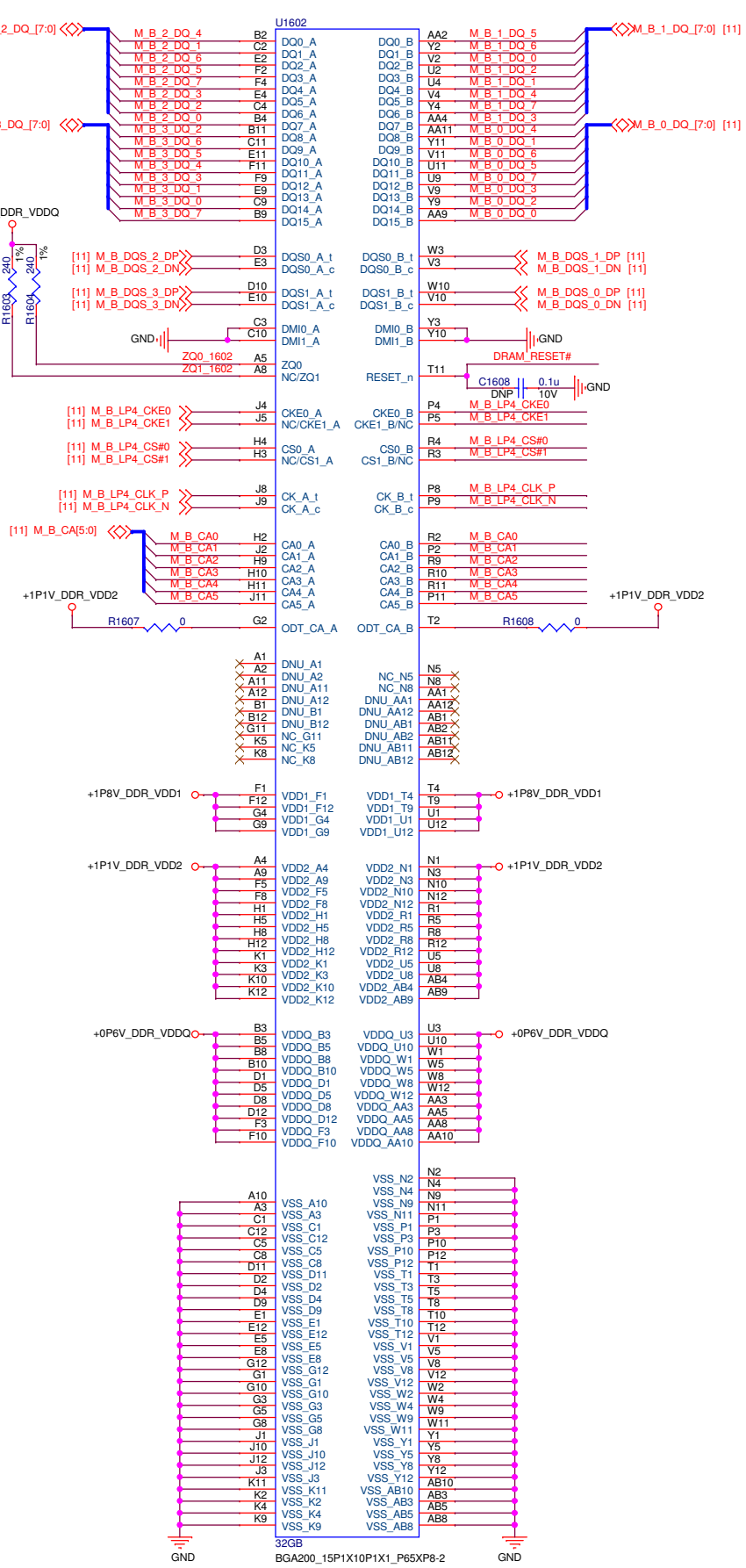
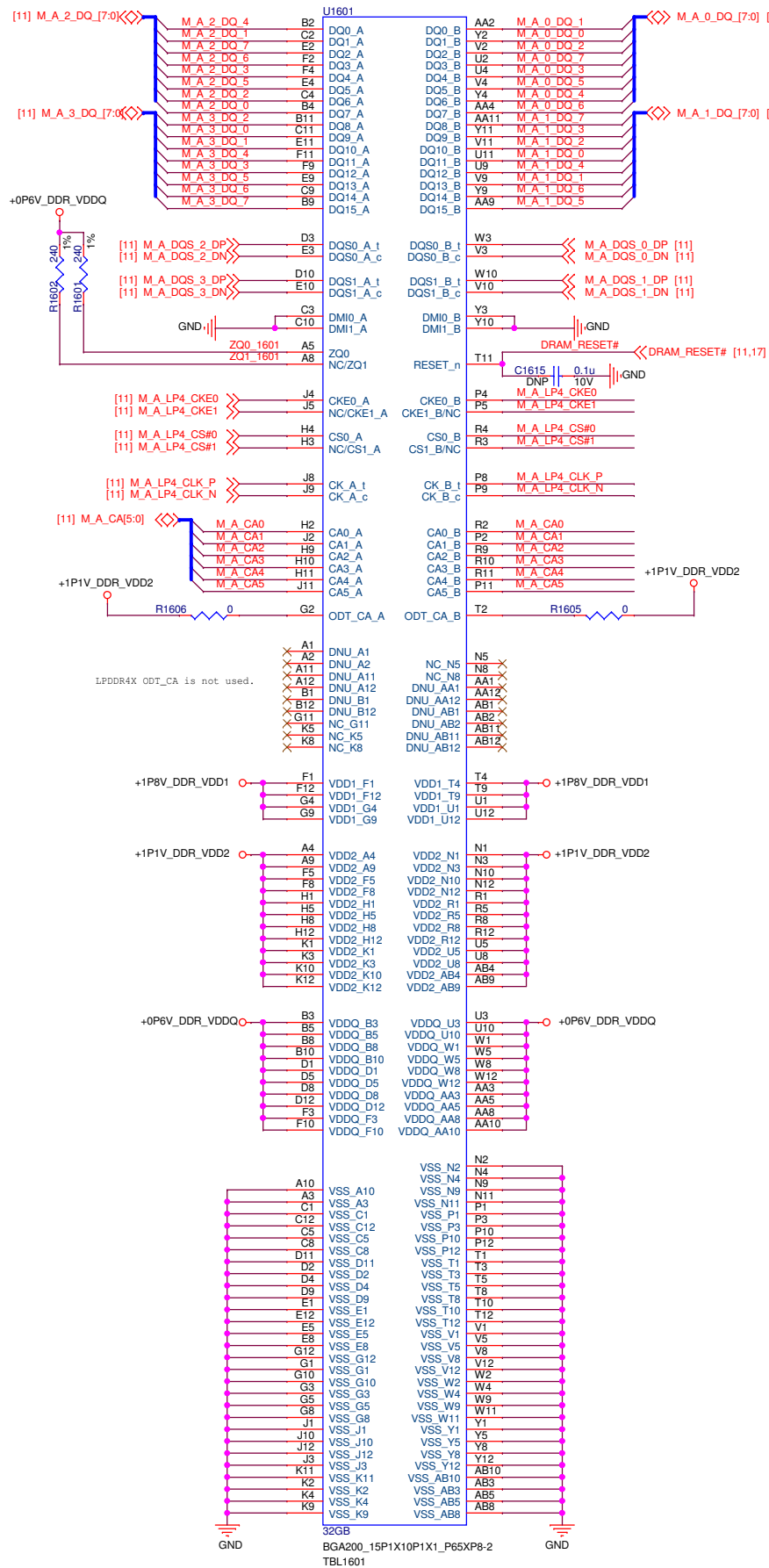
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Size Project Name Rev

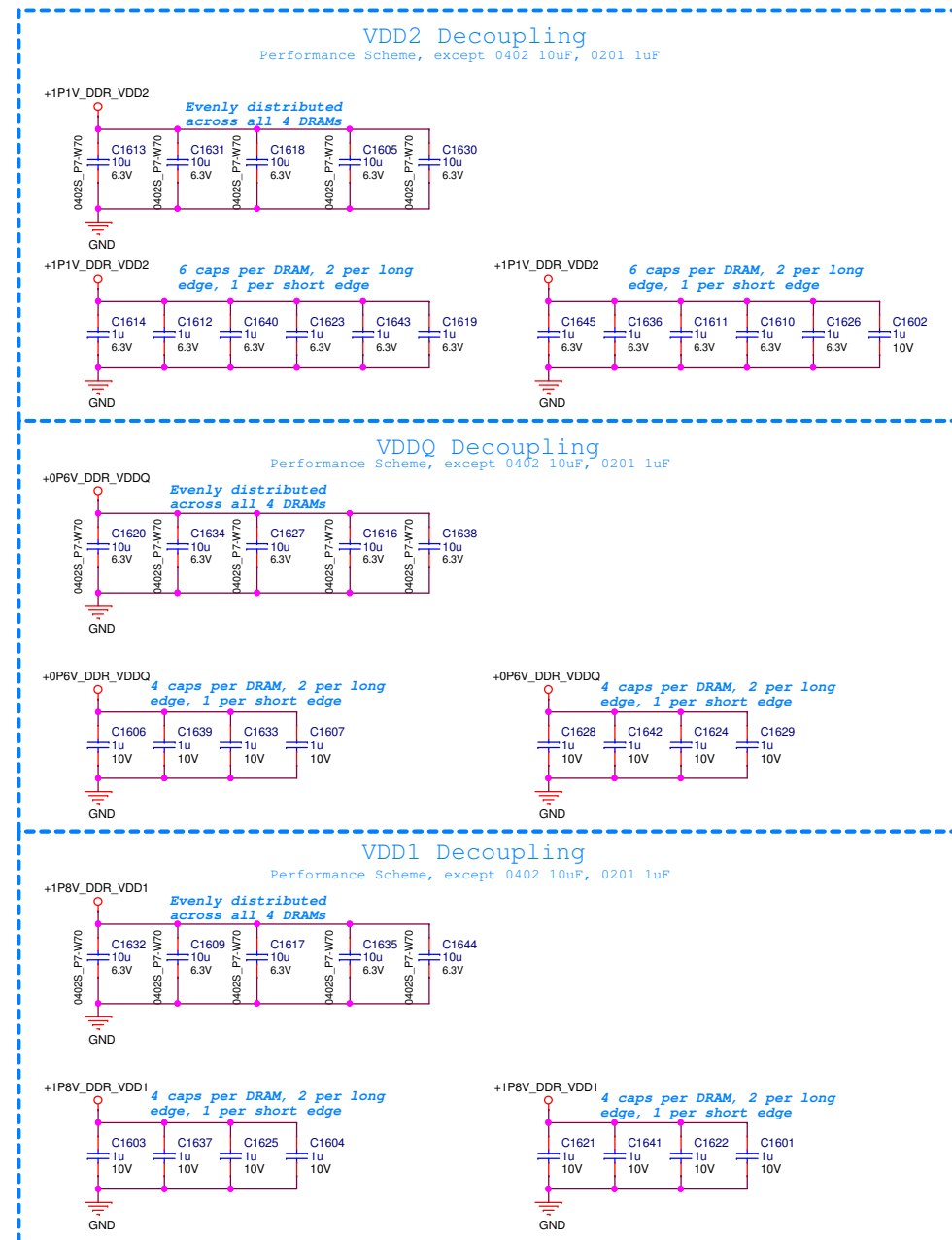
Custom EDAN_A_EV1 1.00

Date: Tuesday, May 21, 2019

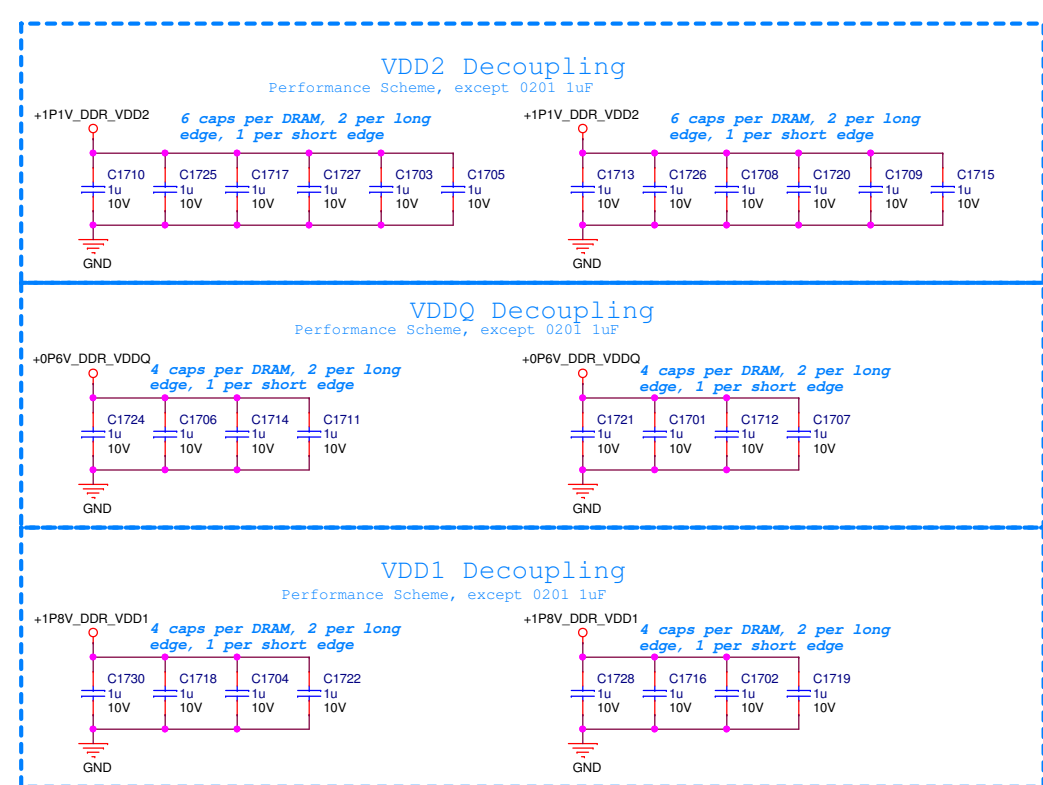
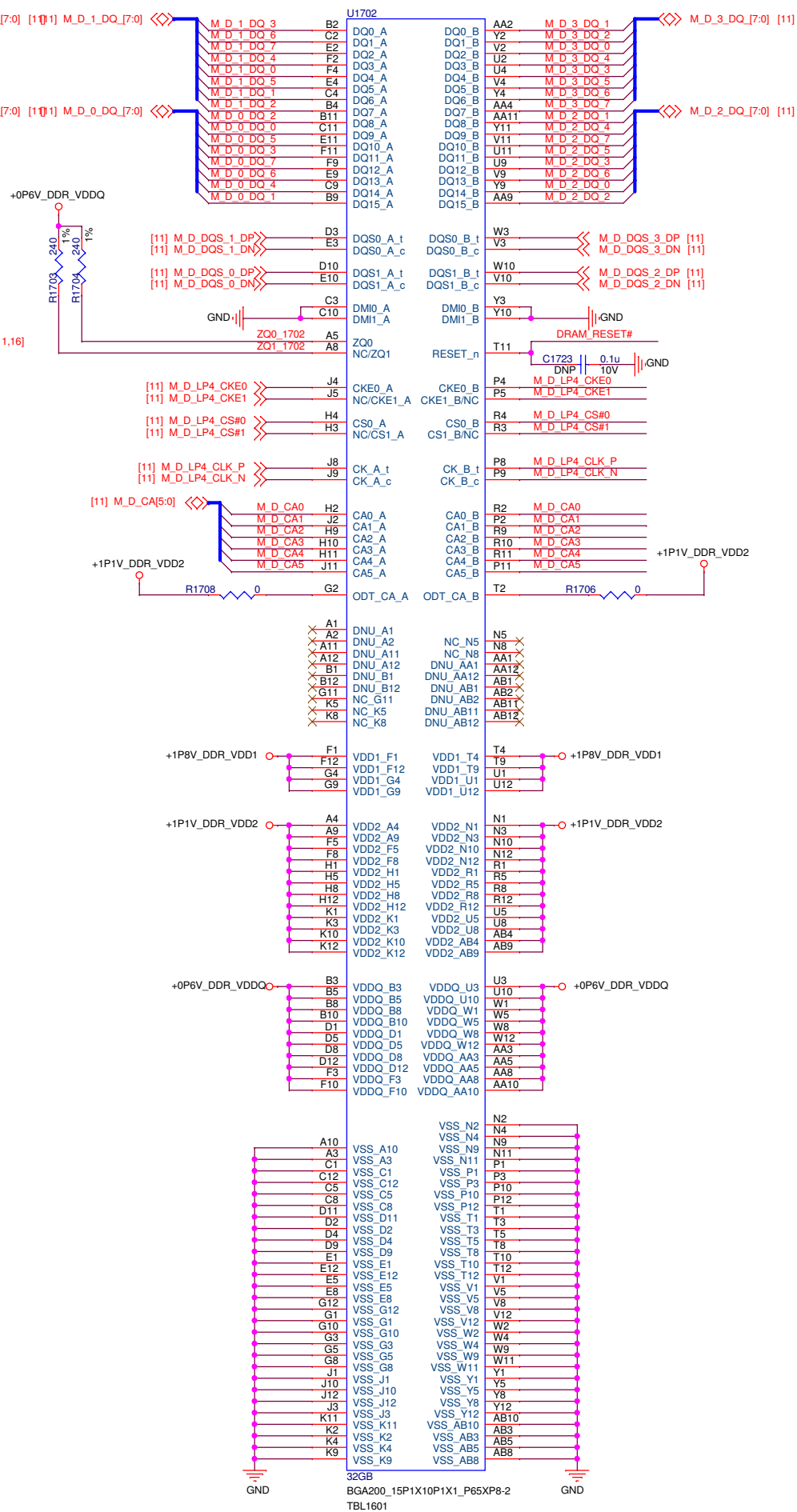
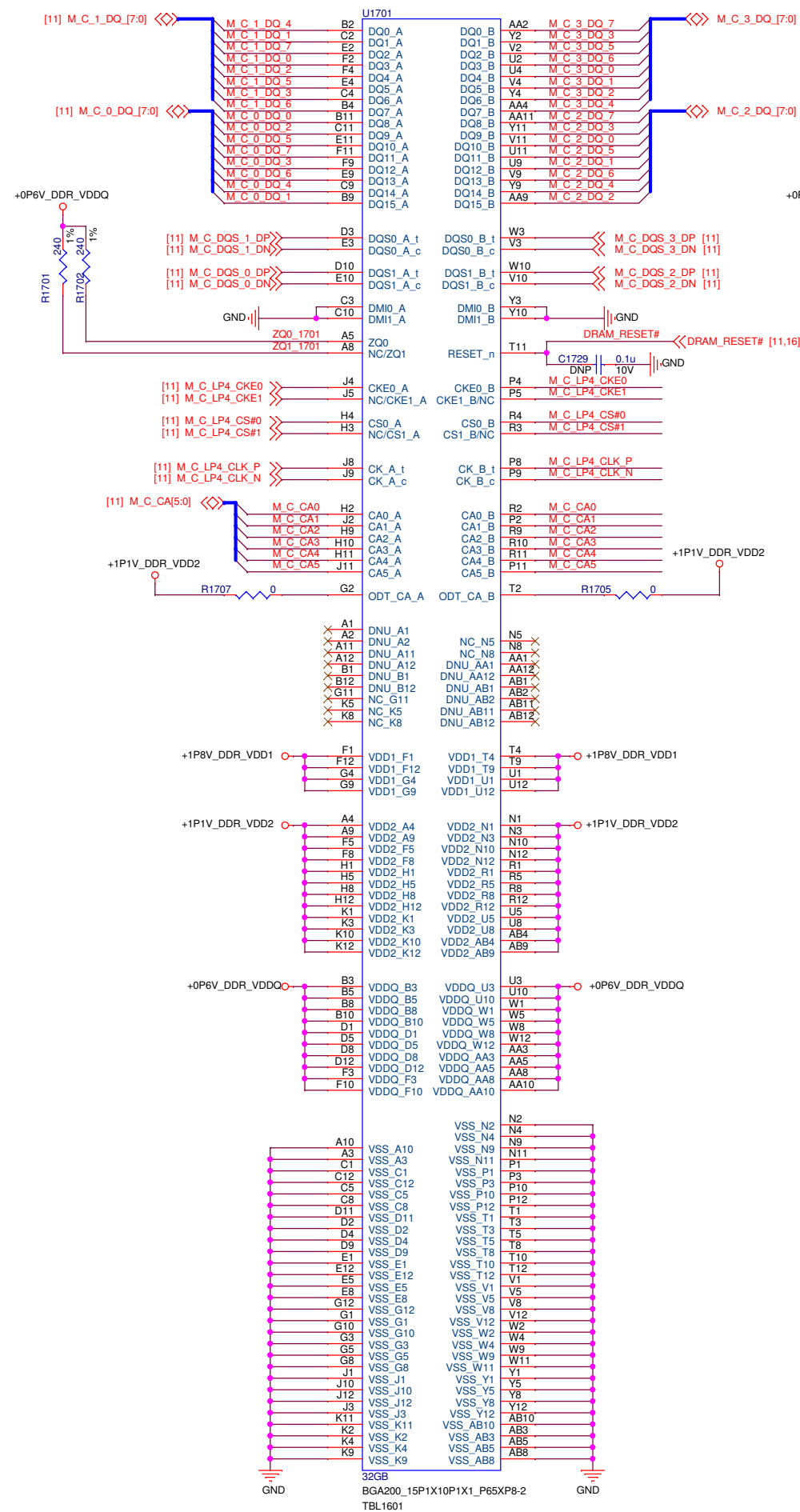
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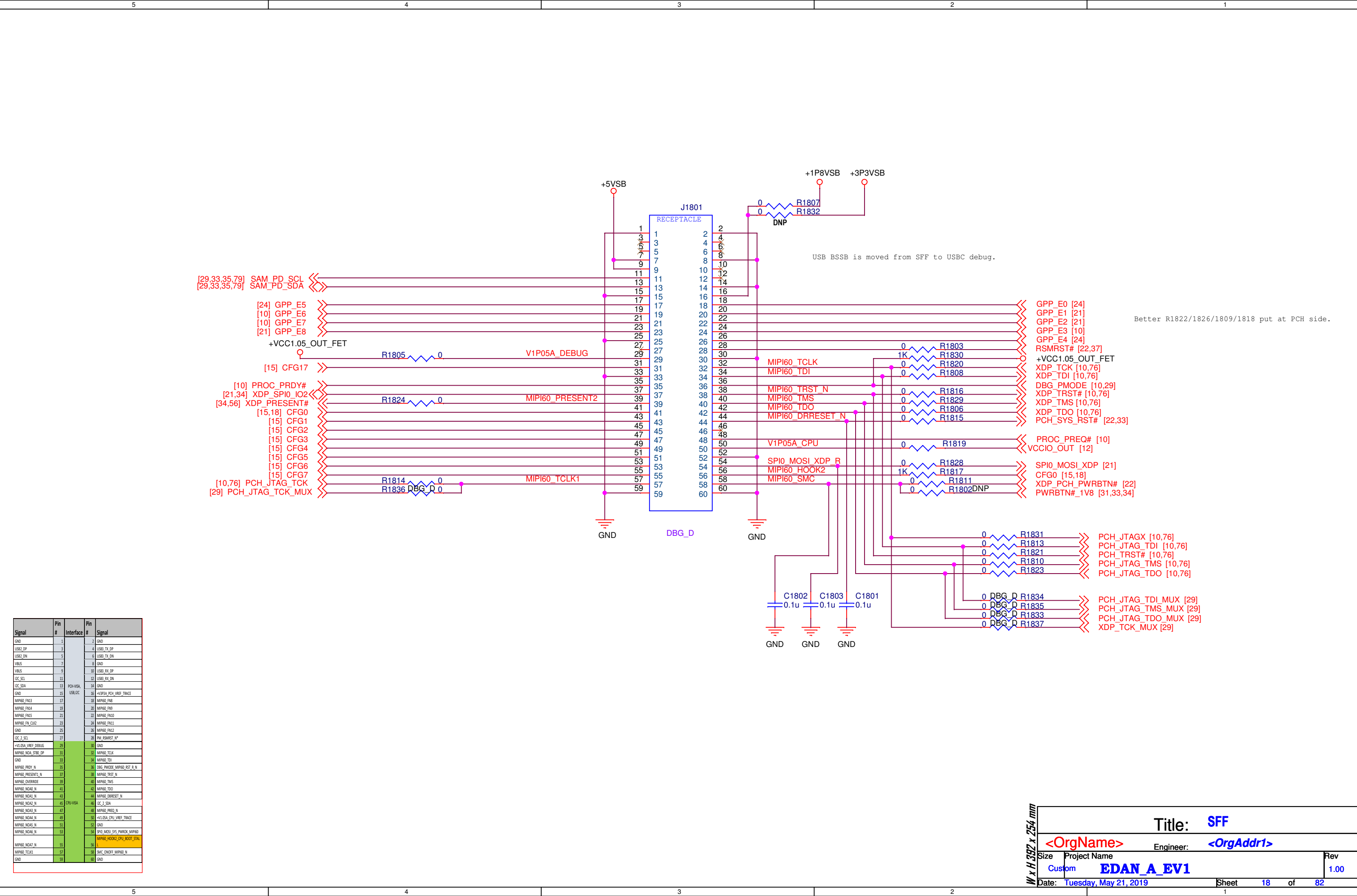


LPDDR4X x32 Performance	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge	24x 1uF (0402)
		evenly distribute among all drams	5x 10uF (0603)
	VDDQ	4 per Dram, 2 per short edge	16x 1uF (0402)
		evenly distribute among all drams	5x 10uF (0603)
	VDD1	4 per dram, 1 per corner (connected to edge and inner BGA)	16x 1uF (0402)
		Evenly distribute	5x 10uF (0603)



MEMORY TABLE 1601			
Manufacturer	MPN	Size	MSPN
Samsung	K4U6E3S4AA-MGCL	16Gb (2GB)	M1100585-001
Samsung	K4UB3D4AA-MGCL	32Gb(4GB)	M1100590-001
Samsung	K4UCE3Q4AA-MGCL	64Gb (8GB)	M1100591-001
Hynix	H9HCNNNBKMLHR-NEE	16Gb (2GB)	M1102096-001
Hynix	H9HCNNNCPMALHR-NEE	32Gb(4GB)	M1102097-001





Signal	Pin #	Interface #	Pin	Signal
GND	1	PCH-VISA USB-DC	2	GND
USB2_DP	3		4	USB2_TX_DP
USB2_DN	5		6	USB2_TX_DN
VBUS	7		8	GND
VBUS	9		10	USB2_RX_DP
DC_SCL	11		12	USB2_RX_DN
DC_SDA	13		14	GND
GND	15		16	+V3P3A_PCH_VREF_TRACE
MIPI60_FIN3	17		18	MIPI60_FIN8
MIPI60_FIN4	19		20	MIPI60_FIN9
MIPI60_FIN5	21		22	MIPI60_FIN10
MIPI60_FIN_CLKD	23		24	MIPI60_FIN11
GND	25		26	MIPI60_FIN12
DC_2_SCL	27		28	PM_RSMRST_N*
+V1P05A_VREF_DEBUG	29		30	GND
MIPI60_NDA_STRO_DP	31	CPU-VISA	32	MIPI60_TCLK
GND	33		34	MIPI60_TDI
MIPI60_PROV_N	35		36	DBG_PMODE_MIP60_RST_R_N
MIPI60_PRESENT1_N	37		38	MIPI60_TRST_IN
MIPI60_OVERRIDE	39		40	MIPI60_TMS
MIPI60_NDA4_N	41		42	MIPI60_TDO
MIPI60_NDA5_N	43		44	MIPI60_DRRESET_N
MIPI60_NDA2_N	45		46	DC_2_SDA
MIPI60_NDA3_N	47		48	MIPI60_PREQ_N
MIPI60_NDA6_N	49		50	+V1P05A_CPU_VREF_TRACE
MIPI60_NDA5_N	51		52	GND
MIPI60_NDA6_N	53		54	SPI0_MOSI_SPS_PWRCK_MIP60
MIPI60_NDA7_N	55		56	MIPI60_HOOK2_CPU_BOOT_STAL
MIPI60_TCLK1	57		58	MIPI60_ONOFF_MIP60_N
GND	59		60	GND

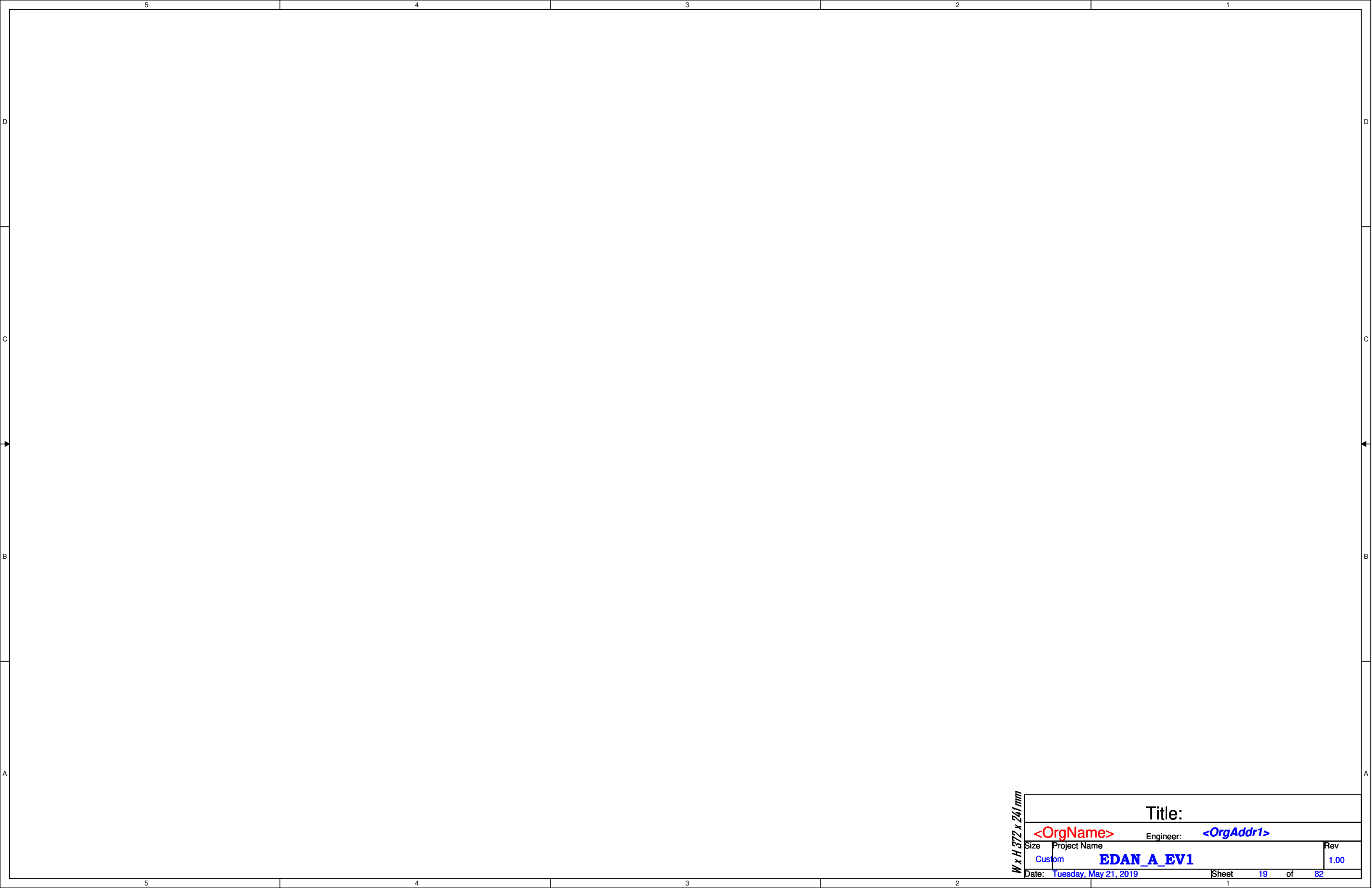
W x H 392 x 254 mm

Title: SFF

<OrgName> Engineer: <OrgAddr1>

Size Project Name Custom EDAN_A_EV1 Rev 1.00

Date: Tuesday, May 21, 2019 Sheet 18 of 82

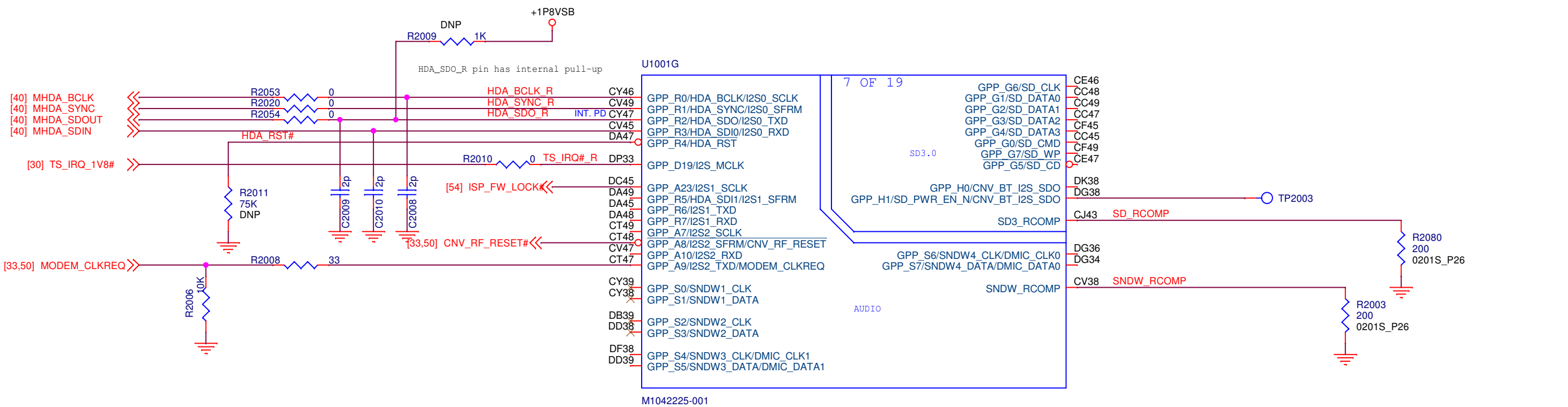
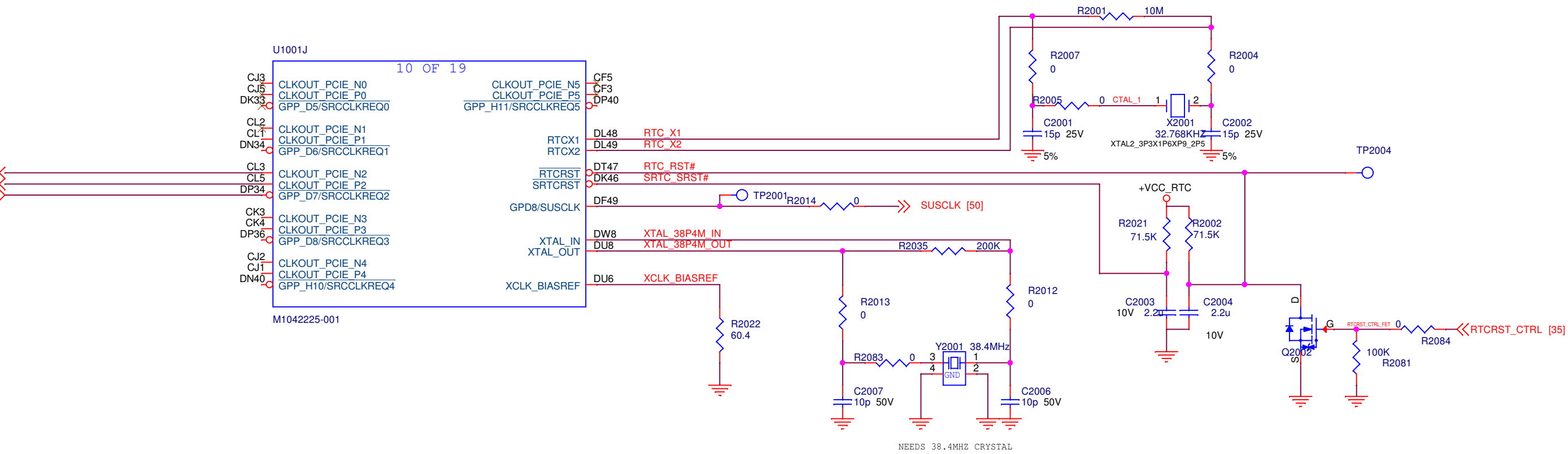


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Size Custom	Project Name EDAN_A_EV1
Date: Tuesday, May 21, 2019	Rev 1.00

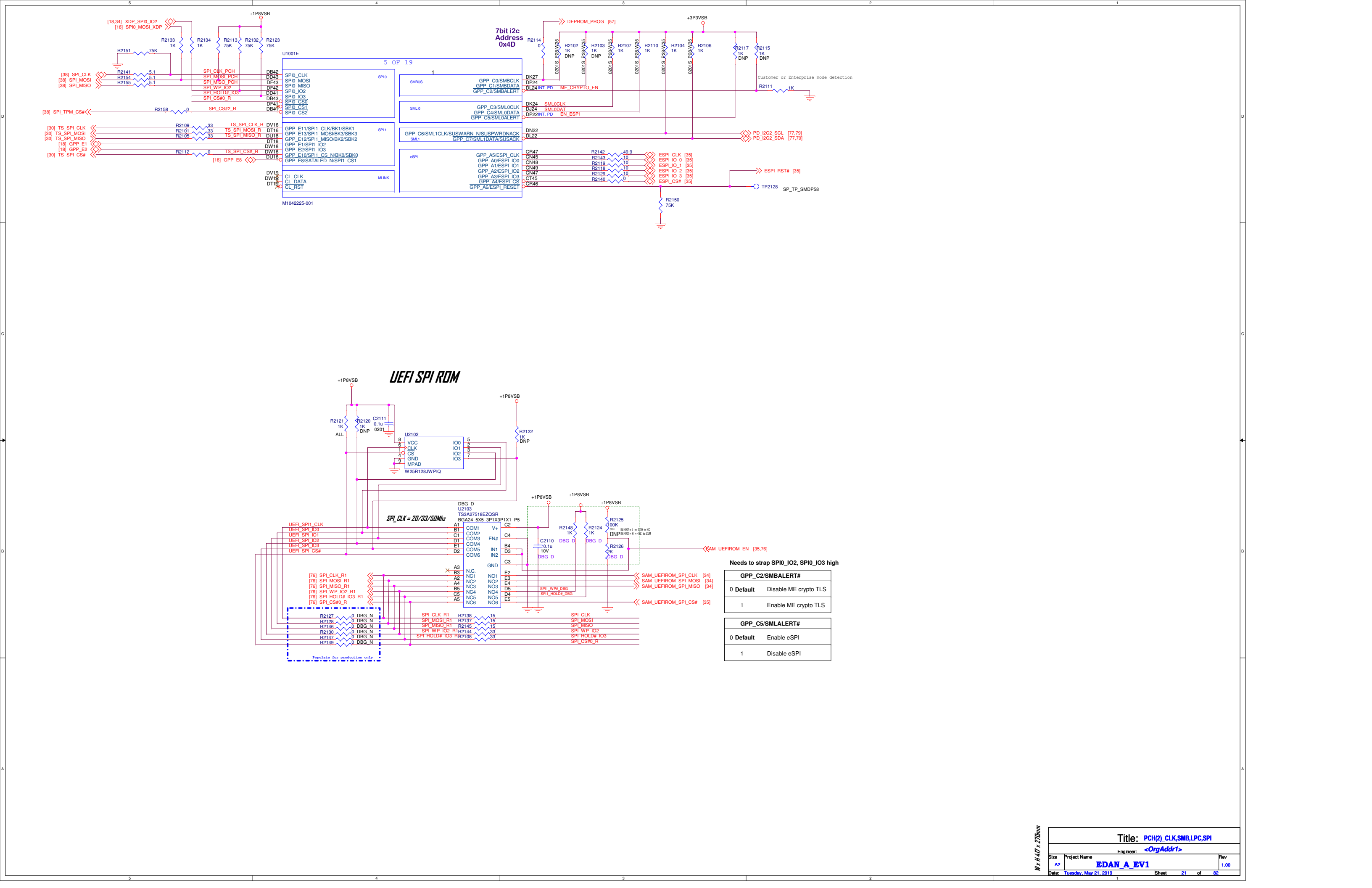
W x H 372 x 241 mm

M.2 SSD

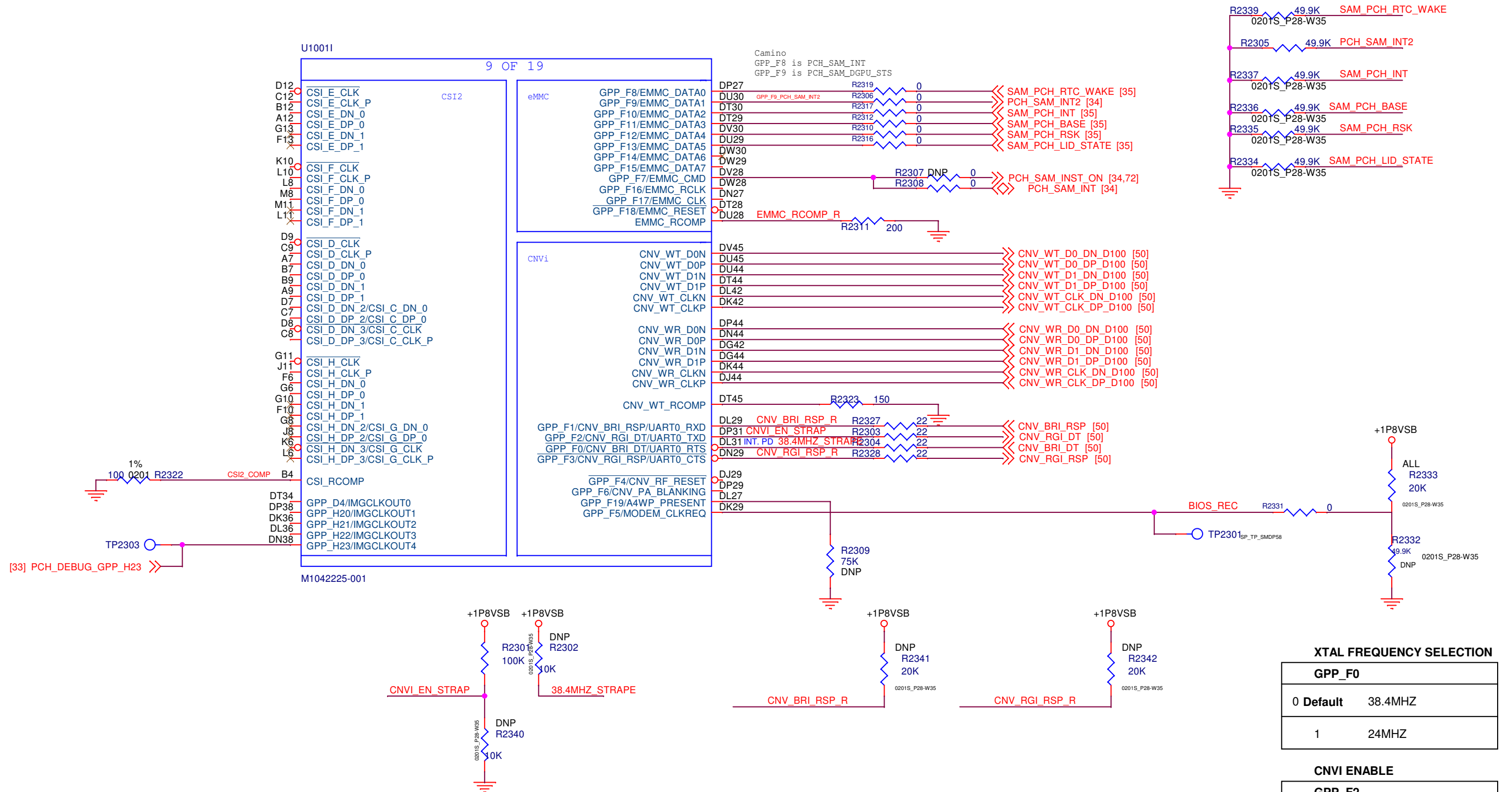
[44] M2_PCIECLK_N
[44] M2_PCIECLK_P
[44] M2_PCIECLK_REQ#



GPP_R2/HDA_SDO	
0 Default	Enable Flash Security
1	Disable Flash Security



Please place testpoints at back of SoC and as close as possible.



XTAL FREQUENCY SELECTION	
GPP_F0	
0 Default	38.4MHZ
1	24MHZ

CNVi ENABLE	
GPP_F2	
0 Default	Integrated CNVi Enabled
1	Integrated CNVi Disabled

PCIE M.2 SSD

[44] PCIE_SSD_RX0_DN
[44] PCIE_SSD_RX0_DP
[44] PCIE_SSD_TX0_DN
[44] PCIE_SSD_TX0_DP

[44] PCIE_SSD_RX1_DN
[44] PCIE_SSD_RX1_DP
[44] PCIE_SSD_TX1_DN
[44] PCIE_SSD_TX1_DP

[44] PCIE_SSD_RX2_DN
[44] PCIE_SSD_RX2_DP
[44] PCIE_SSD_TX2_DN
[44] PCIE_SSD_TX2_DP

[44] PCIE_SSD_RX3_DN
[44] PCIE_SSD_RX3_DP
[44] PCIE_SSD_TX3_DN
[44] PCIE_SSD_TX3_DP

[18] GPP_E0
[45] USBA_OVCUR#
[79] TCP0_OC#
[18] GPP_E4
[18] GPP_E5
[57,76] TCON_VENDOR_ID
[33,50] BT_DISABLE#
[33,50] WLAN_DISABLE#

R2401 100
0201S_P28-W35

+1P8VSB
0201S P28-W35 R2410 49.9K TCON_VENDOR_ID

U1001H
8 OF 19

CV7
CV6
DD3
DD5

CT6
CT7
DA3
DA5

CP7
CP6
DA2
DA1

CM7
CM6
CY3
CY4

CK7
CK6
CW2
CW1

CJ6
CJ7
CW5
CW3

CG7
CG6
CT3
CT5

CE6
CE7
CT2
CT1

CC5
CC6
CR3
CR4

CA6
CA5
CP1
CP2

DW12
CR42
CR43

DW14
CT43

DU12
DU11
CV48

DT38
DW38
DV38
DU38

M1042225-001

PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP

PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP

PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP

PCIE11_RXN/SATA0_RXN
PCIE11_RXP/SATA0_RXP
PCIE11_TXN/SATA0_TXN
PCIE11_TXP/SATA0_TXP

PCIE12_RXN/SATA1A_RXN
PCIE12_RXP/SATA1A_RXP
PCIE12_TXN/SATA1A_TXN
PCIE12_TXP/SATA1A_TXP

PCIE13_RXN
PCIE13_RXP
PCIE13_TXN
PCIE13_TXP

PCIE14_RXN
PCIE14_RXP
PCIE14_TXN
PCIE14_TXP

PCIE15_RXN/SATA1B_RXN
PCIE15_RXP/SATA1B_RXP
PCIE15_TXN/SATA1B_TXN
PCIE15_TXP/SATA1B_TXP

PCIE16_RXN/SATA2_RXN
PCIE16_RXP/SATA2_RXP
PCIE16_TXN/SATA2_TXN
PCIE16_TXP/SATA2_TXP

GPP_E0/SATAXPCE0/SATAGP0
GPP_A12/SATAXPCE1/SATAGP1
GPP_A13/SATAXPCE2/SATAGP2

GPP_E9/USB_OC0
GPP_A16/USB_OC3

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_A11/SATA_DEVSLP2

GPP_H12/M2_SKT2_CFG0
GPP_H13/M2_SKT2_CFG1
GPP_H14/M2_SKT2_CFG2
GPP_H15/M2_SKT2_CFG3

PCIE_RCOMPN DN1
PCIE_RCOMP DN3

PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP

PCIE2_RXN/USB31_2_RXN
PCIE2_RXP/USB31_2_RXP
PCIE2_TXN/USB31_2_TXN
PCIE2_TXP/USB31_2_TXP

PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP

PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP

PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP

PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP

USB2N_1
USB2P_1

USB2N_2
USB2P_2

USB2N_3
USB2P_3

USB2N_4
USB2P_4

USB2N_5
USB2P_5

USB2N_6
USB2P_6

USB2N_7
USB2P_7

USB2N_8
USB2P_8

USB2N_9
USB2P_9

USB2N_10
USB2P_10

USB_ID

USB_VBUSSENSE

USB2_COMP

UFS_RESET

PCIE1_RXN/USB31_1_RXN
PCIE1_RXP/USB31_1_RXP
PCIE1_TXN/USB31_1_TXN
PCIE1_TXP/USB31_1_TXP

PCIE2_RXN/USB31_2_RXN
PCIE2_RXP/USB31_2_RXP
PCIE2_TXN/USB31_2_TXN
PCIE2_TXP/USB31_2_TXP

PCIE3_RXN/USB31_3_RXN
PCIE3_RXP/USB31_3_RXP
PCIE3_TXN/USB31_3_TXN
PCIE3_TXP/USB31_3_TXP

PCIE4_RXN/USB31_4_RXN
PCIE4_RXP/USB31_4_RXP
PCIE4_TXN/USB31_4_TXN
PCIE4_TXP/USB31_4_TXP

PCIE5_RXN/USB31_5_RXN
PCIE5_RXP/USB31_5_RXP
PCIE5_TXN/USB31_5_TXN
PCIE5_TXP/USB31_5_TXP

PCIE6_RXN/USB31_6_RXN
PCIE6_RXP/USB31_6_RXP
PCIE6_TXN/USB31_6_TXN
PCIE6_TXP/USB31_6_TXP

USB2N_1
USB2P_1

USB2N_2
USB2P_2

USB2N_3
USB2P_3

USB2N_4
USB2P_4

USB2N_5
USB2P_5

USB2N_6
USB2P_6

USB2N_7
USB2P_7

USB2N_8
USB2P_8

USB2N_9
USB2P_9

USB2N_10
USB2P_10

USB_ID

USB_VBUSSENSE

USB2_COMP

UFS_RESET

DJ8
DJ6
DJ2
DJ1

DG9
DG7
DJ3
DJ5

DE7
DE9
DF3
DF5

DC7
DC9
DF2
DF1

DA6
DA7
DE4
DE3

CY7
CY6
DD1
DD2

DN8
DP8

DK11
DJ11

DP13
DN13

DK10
DJ10

DL5
DL3

DP11
DN11

DK13
DJ13

DN6
DP6

DL2
DL1

DP10
DN10

DL6
DL11

DN5
CD3

TP2401

USB3_SL1_RXN4 [71]
USB3_SL1_RXP4 [71]
USB3_SL1_TXN4 [71]
USB3_SL1_TXP4 [71]

USB3_USBA_RX_DN [45]
USB3_USBA_RX_DP [45]
USB3_USBA_TX_DN [45]
USB3_USBA_TX_DP [45]

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USB2_SL1_DP [71]

USB2_USBA_DN [45]
USB2_USBA_DP [45]

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USB2_TCP0_DP [77]

CAM_USB_DM_SOC [54]
CAM_USB_DP_SOC [54]

10K R2405
10K R2408
R2402 113

USB3 SL40

USB3 TYPE A AND BSSB

USB2 SL40

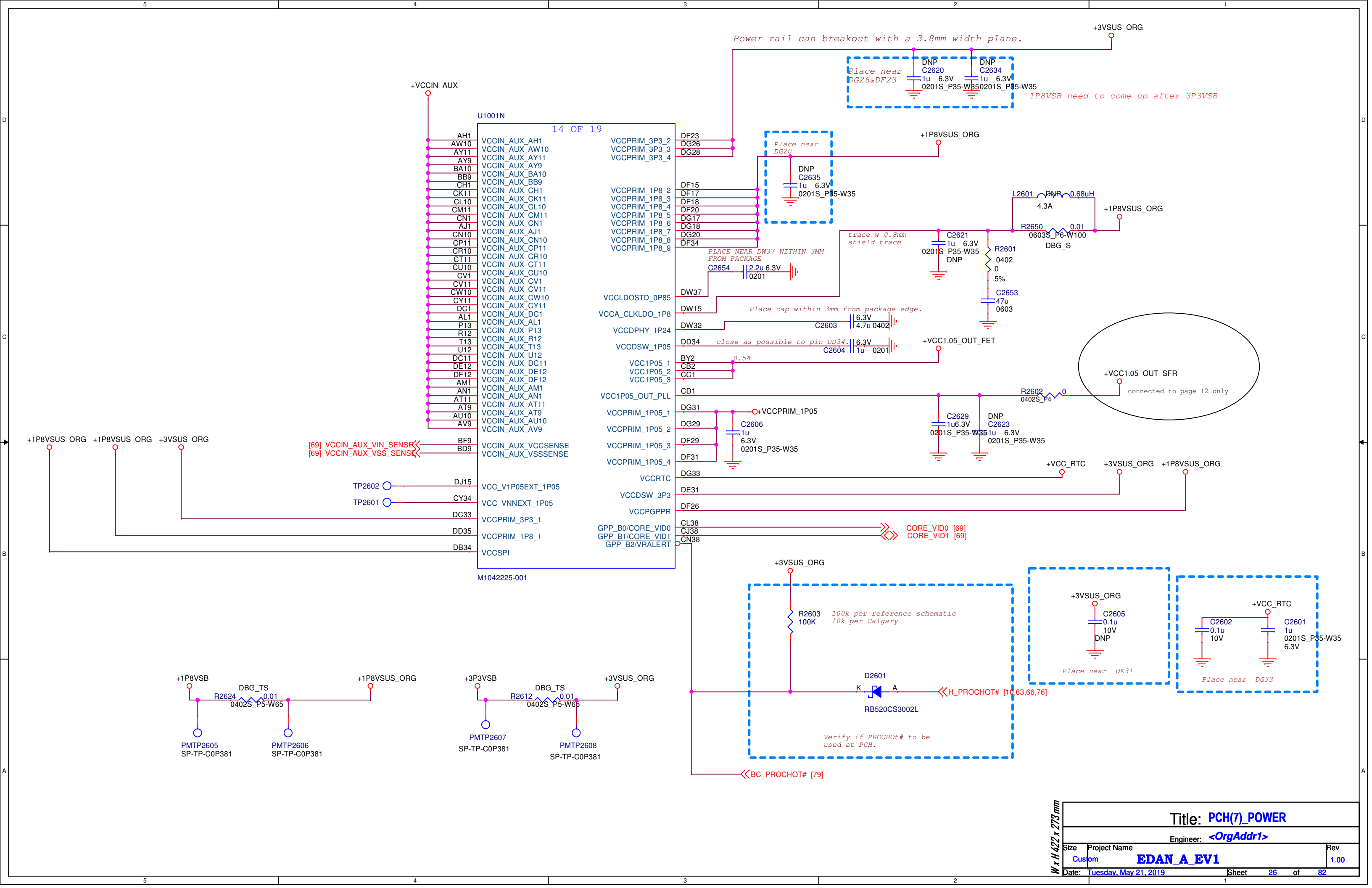
USB2 USB-A PORT

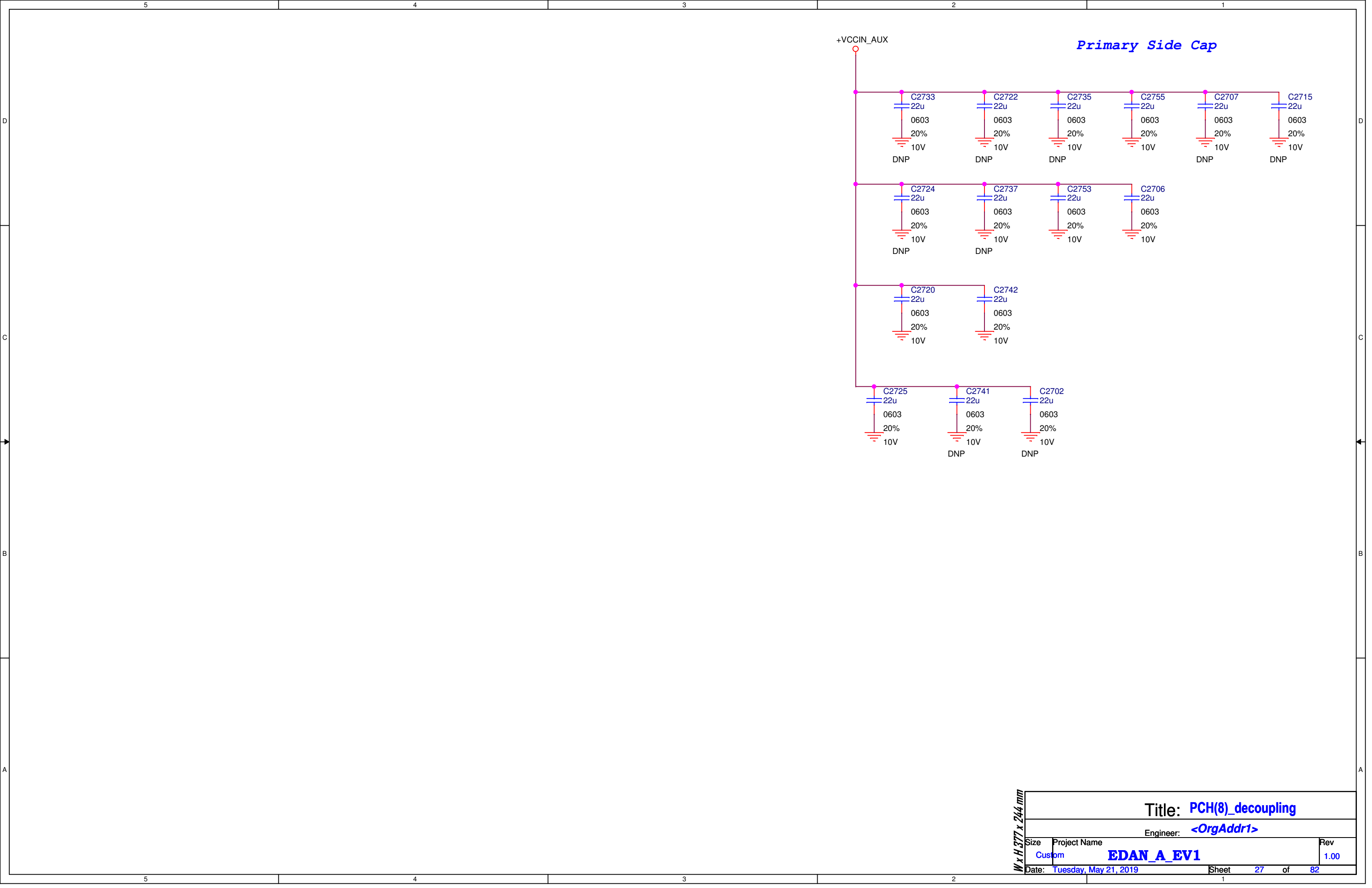
USB2 USB-C PORT1

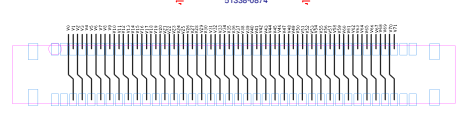
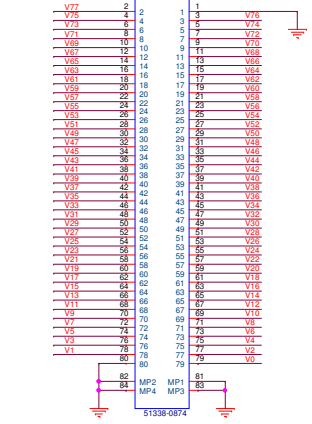
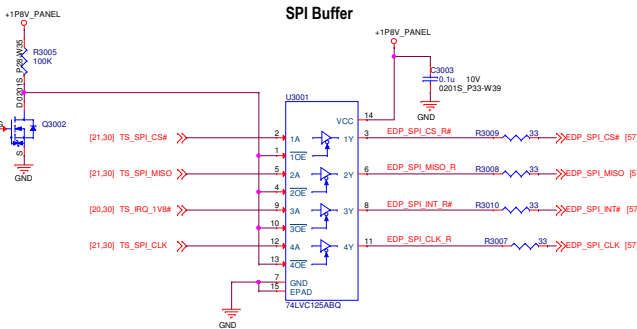
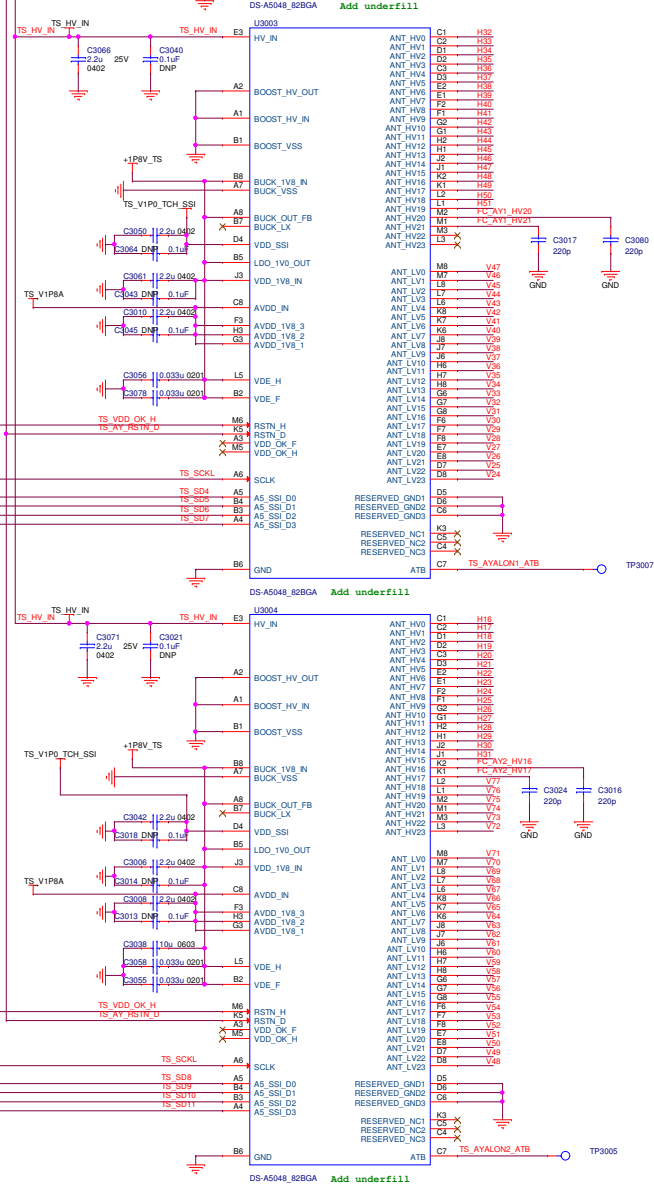
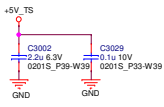
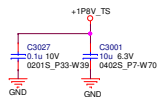
USB2 Camera

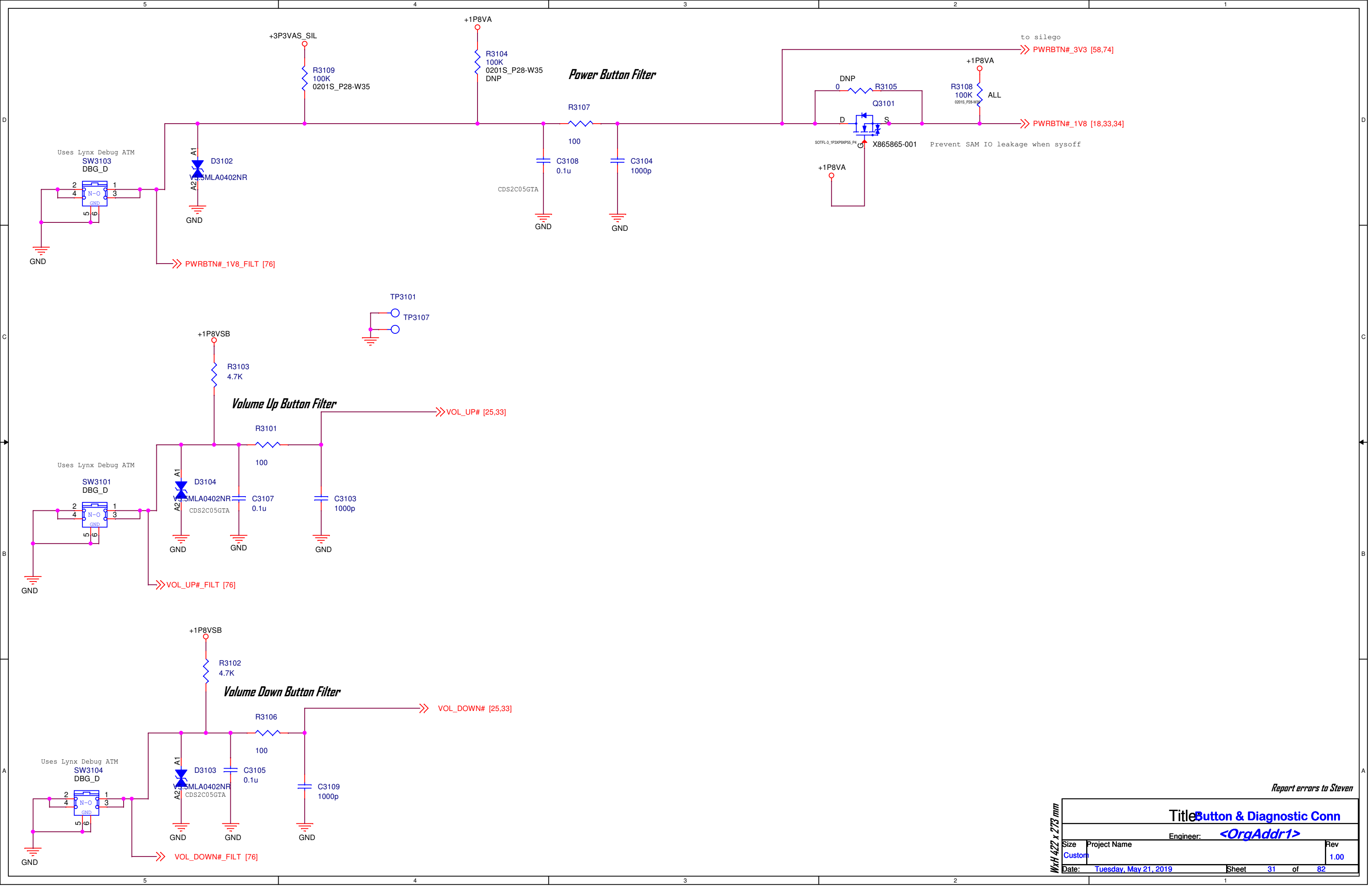
W x H 412 x 267 mm

Title: PCH(5)_PCIE,USB		
Engineer: <OrgAddr1>		
Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00
Date:	Tuesday, May 21, 2019	Sheet 24 of 82



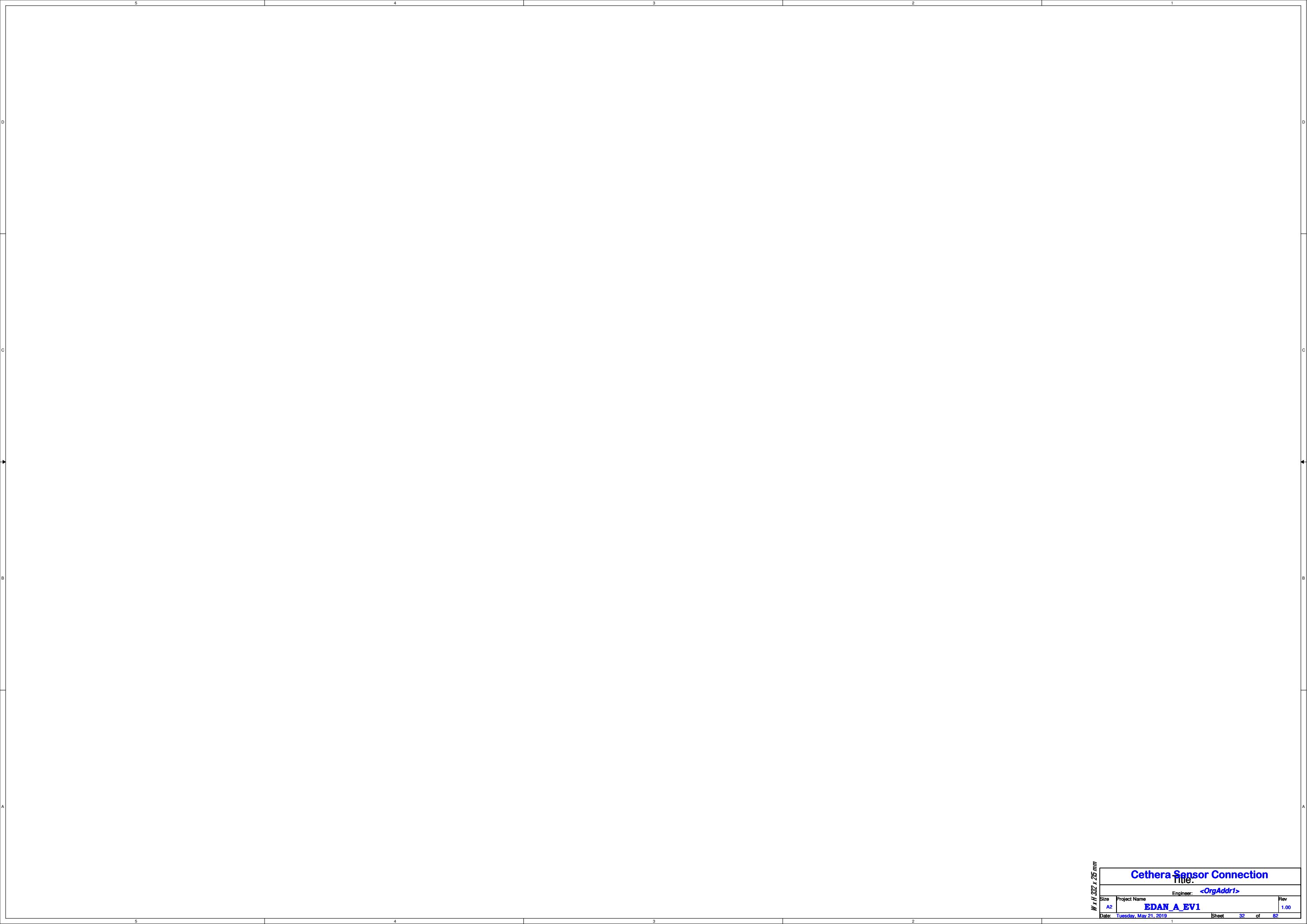




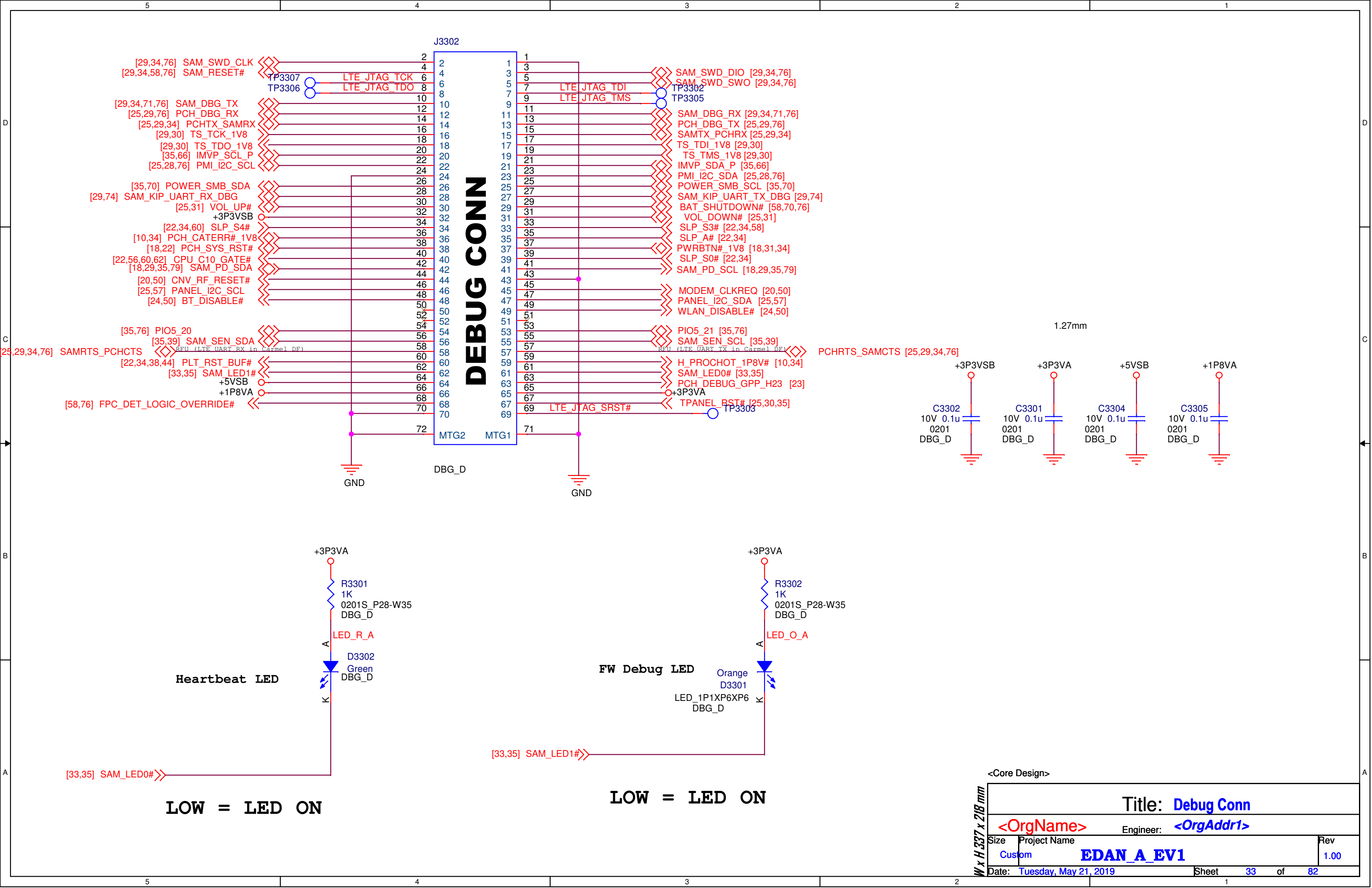


Title: Button & Diagnostic Conn			
Size: Custom		Engineer: <OrgAddr1>	Rev: 1.00
Date: Tuesday, May 21, 2019	Sheet: 31	of: 82	

Report errors to Steven

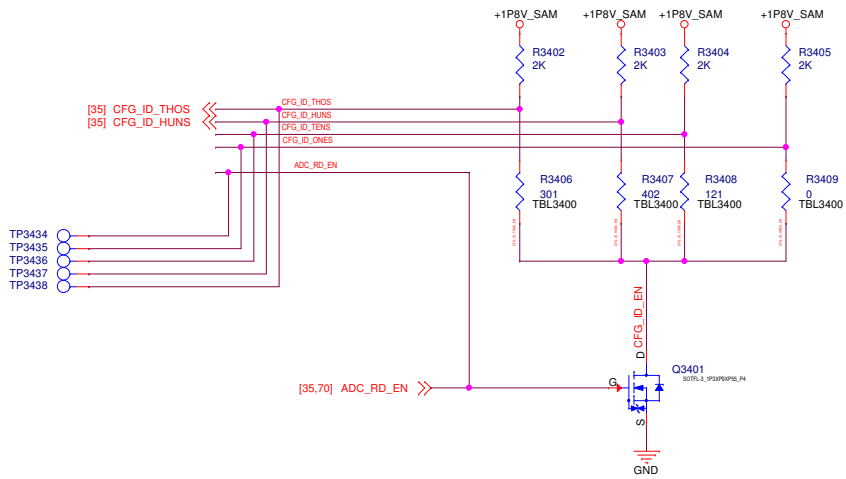
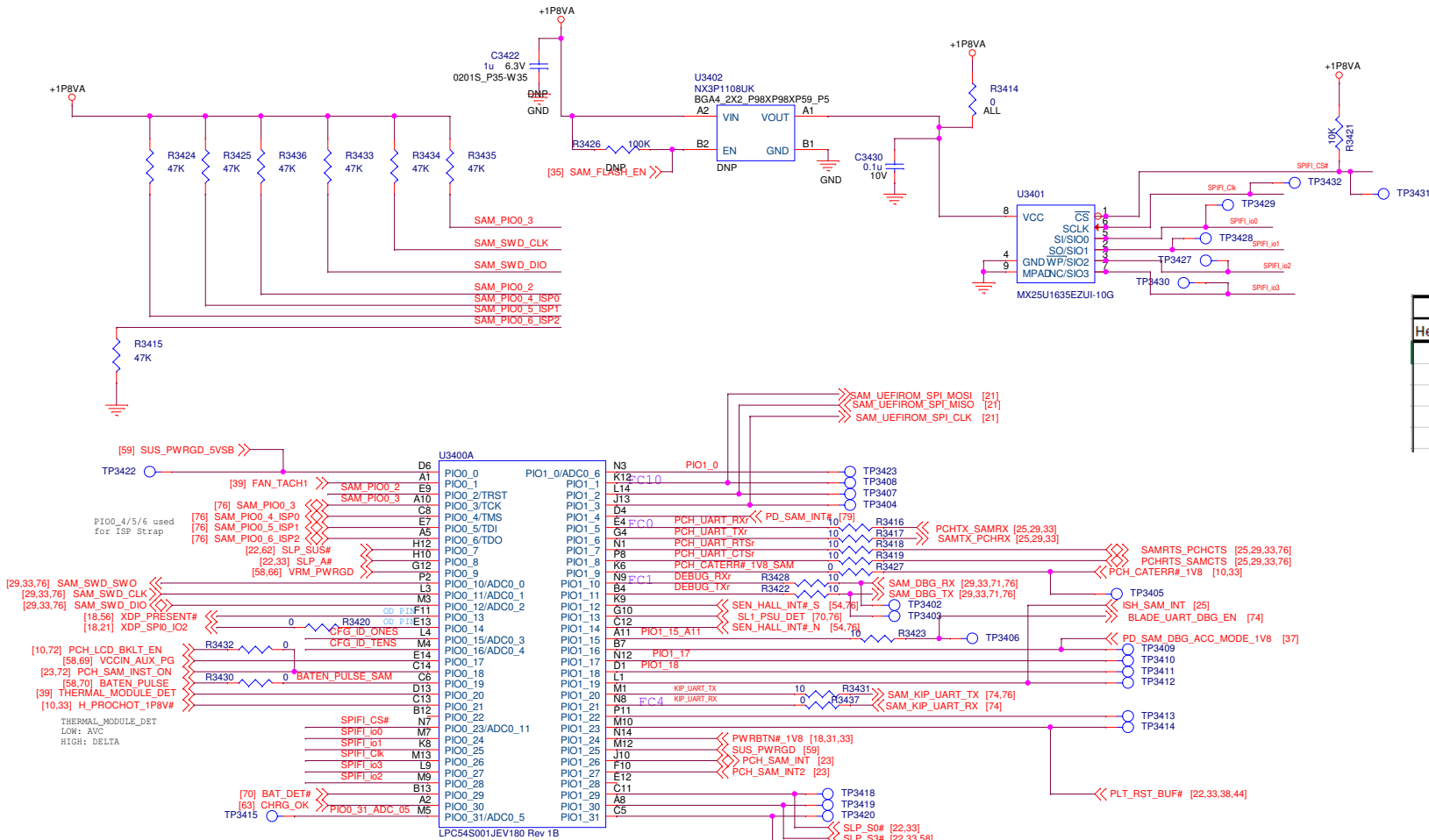
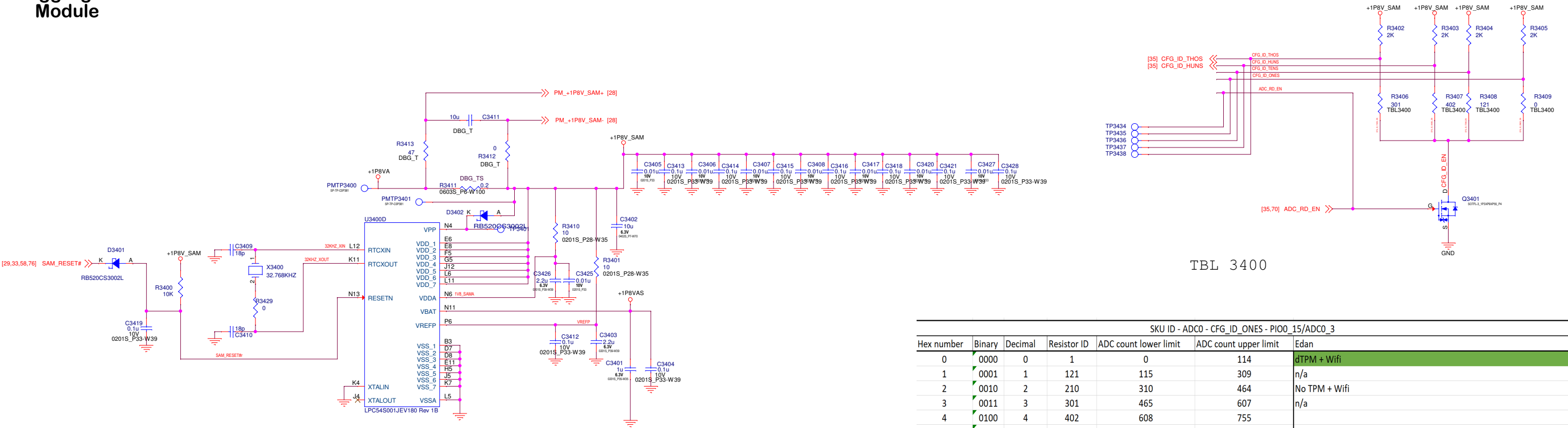


W x H 532 x 295 mm			
Title: Cethera Sensor Connection			
Engineer: <OrgAddr1>			
Size	Project Name	Rev	
A2	EDAN_A_EV1	1.00	
Date:	Tuesday, May 21, 2019	Sheet	32 of 82



System
Aggregator
Module

Configuration ID TBD



TBL 3400

SKU ID - ADC0 - CFG_ID_ONES - PIO0_15/ADC0_3						
Hex number	Binary	Decimal	Resistor ID	ADC count lower limit	ADC count upper limit	Edan
0	0000	0	1	0	114	dTPM + Wifi
1	0001	1	121	115	309	n/a
2	0010	2	210	310	464	No TPM + Wifi
3	0011	3	301	465	607	n/a
4	0100	4	402	608	755	
5	0101	5	510	756	904	
6	0110	6	634	905	1078	
7	0111	7	806	1079	1271	
8	1000	8	1000	1272	1485	Reserved for SW ID
9	1001	9	1300	1486	1756	n/a
A	1010	10	1740	1757	2060	Reserved for SW ID
B	1011	11	2370	2061	2398	n/a

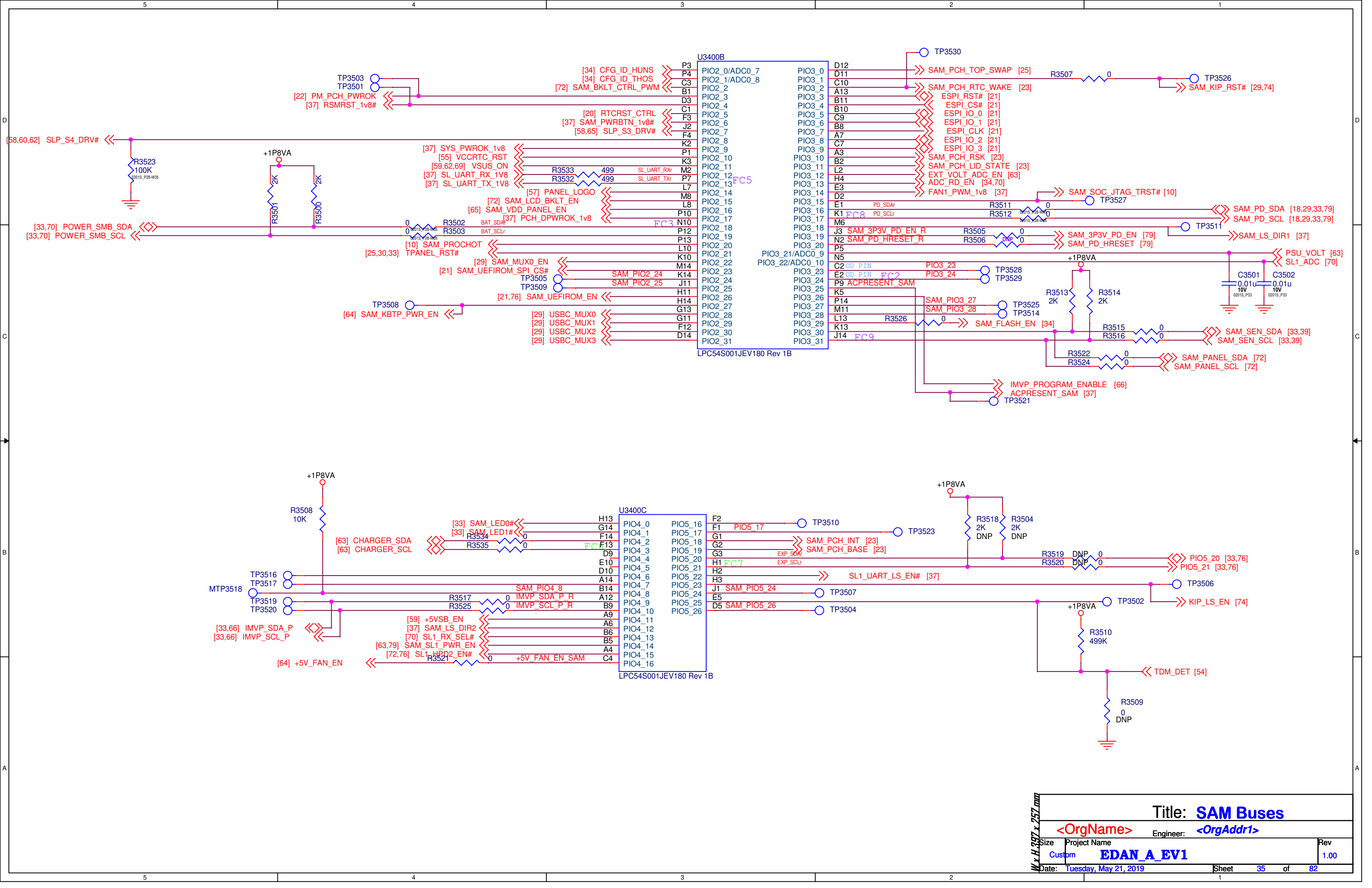
Memory ID - ADC1 - CFG_ID_TENS - PIO0_16/ADC0_4						
Hex number	binary	decimal	Resistor ID	ADC count lower limit	ADC count upper limit	Edan
0	0000	0	1	0	114	LP4x_2GB_K4U6E3S4AA-MGCL_SAMSUNG_M1100585-001
1	0001	1	121	115	309	LP4x_4GB_K4UBE3D4AA-MGCL_SAMSUNG_M1100590-001
2	0010	2	210	310	464	LP4x_8GB_K4UCE3Q4AA-MGCL_SAMSUNG_M1100591-001
3	0011	3	301	465	607	
4	0100	4	402	608	755	
5	0101	5	510	756	904	LP4x_2GB_H9HCNNNBKMLHR-NEE_Hynix_M1102096-001
6	0110	6	634	905	1078	LP4x_4GB_H9HCNNNCPMALHR-NEE_Hynix_M1102097-001

Build ID - ADC2 - CFG_ID_HUNS - PIO2_0/ADC0_7						
Hex number	binary	decimal	Resistor ID	ADC count lower limit	ADC count upper limit	Edan
0	0000	0	1	0	114	EV1
1	0001	1	121	115	309	EV1.1
2	0010	2	210	310	464	EV1.5
3	0011	3	301	465	607	EV2
4	0100	4	402	608	755	DV

Program ID - ADC3 - CFG_ID_THOS - PIO2_1/ADC0_8						
Hex number	binary	decimal	Resistor ID	ADC count lower limit	ADC count upper limit	
0	0000	0	1	0	114	
1	0001	1	121	115	309	
2	0010	2	210	310	464	
3	0011	3	301	465	607	Edan

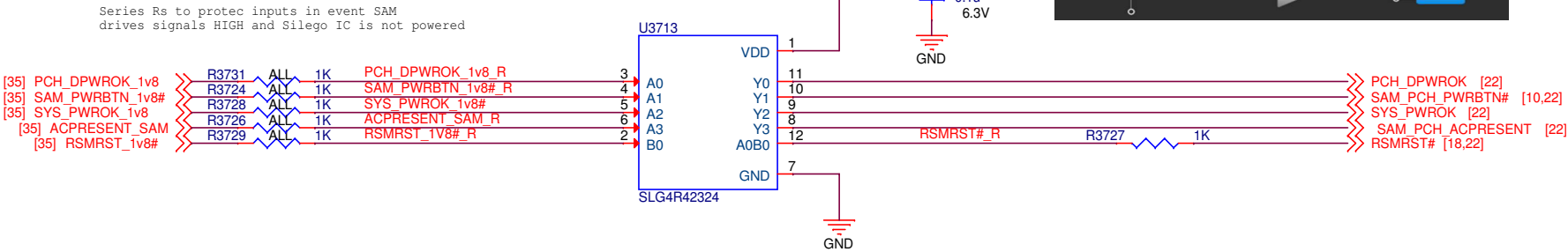
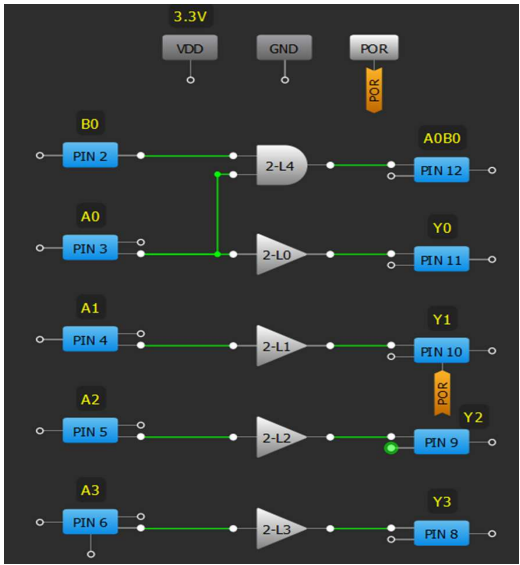
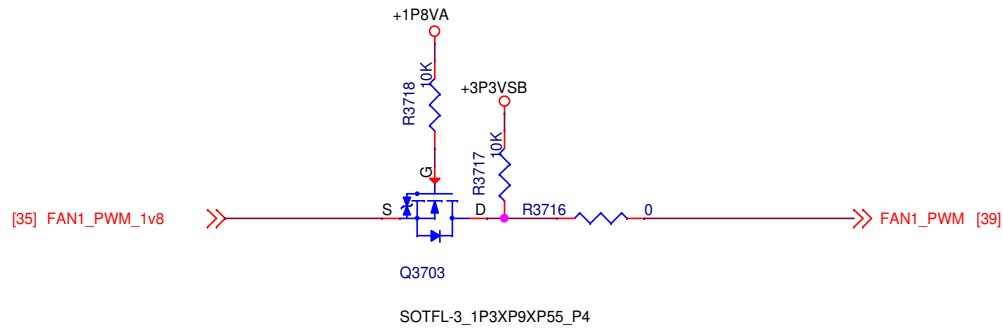
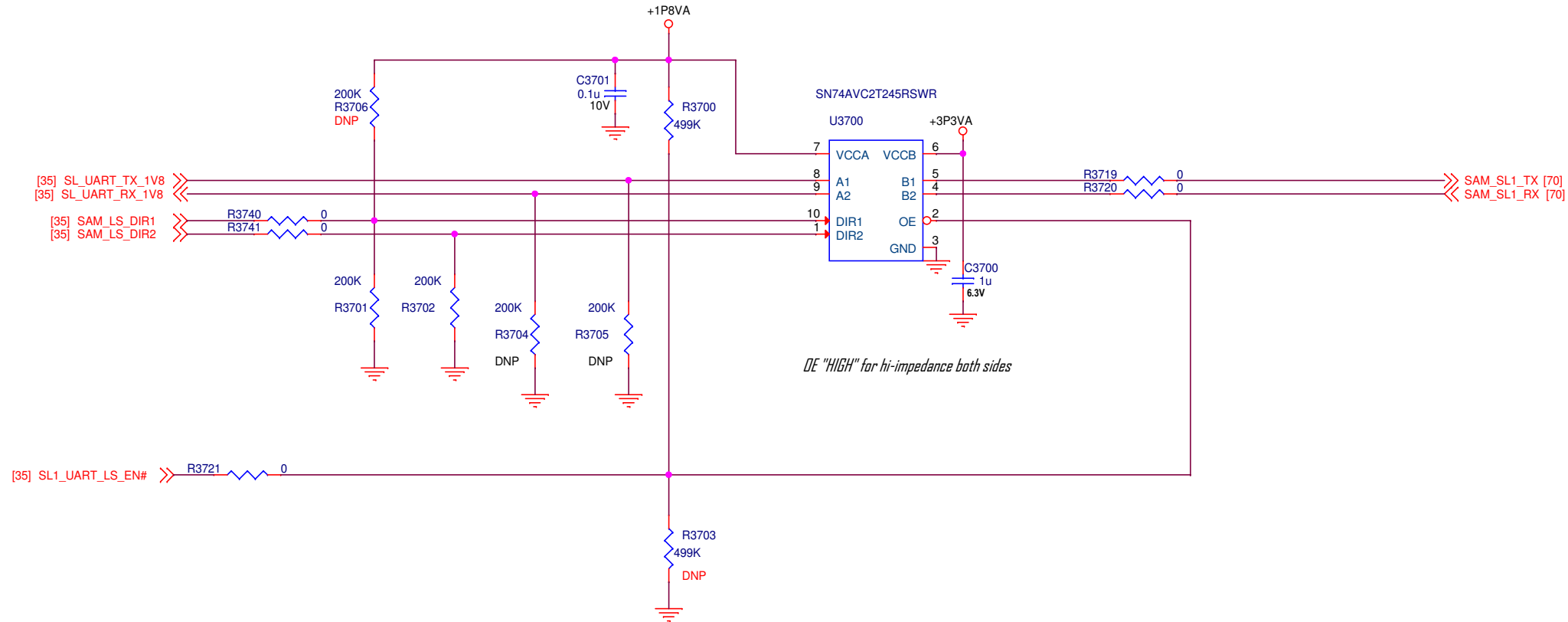
W x H 422 x 310 mm

SAM Power, ADC, & Debug			
Title		Rev	
<OrgName>		Engineer: <OrgAddr1>	
Size	A2	Project Name	EDAN_A_EV1
Date	Tuesday, May 21, 2019	Sheet	34 of 82





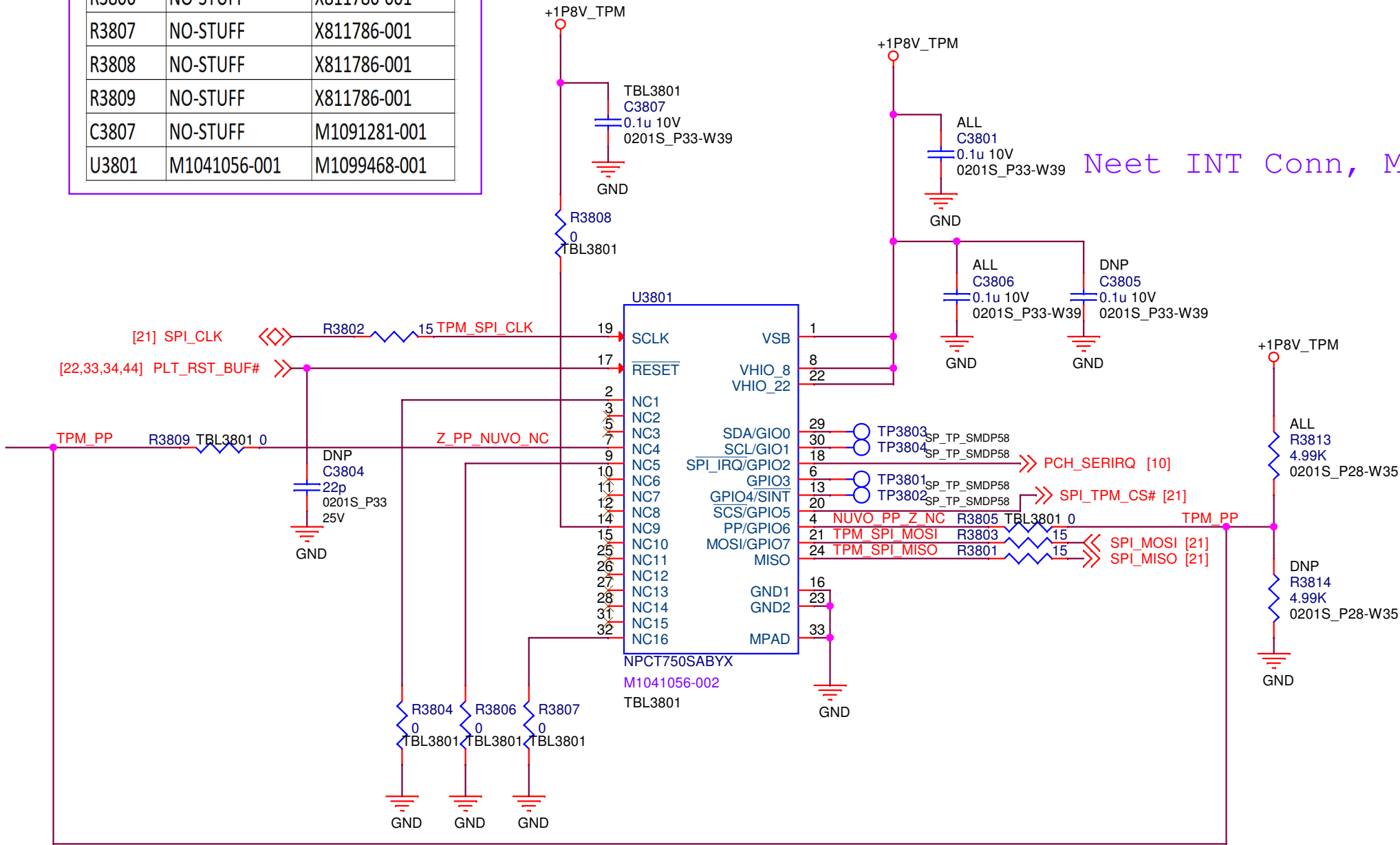
		Title: <i>Blank</i>	
<OrgName>		Engineer: <OrgAddr>	
Size	Project Name		Rev
A1	EDAN A EV1		1.00
Date: Tuesday, May 21, 2019		Sheet	25 of 25



Trusted Platform Module

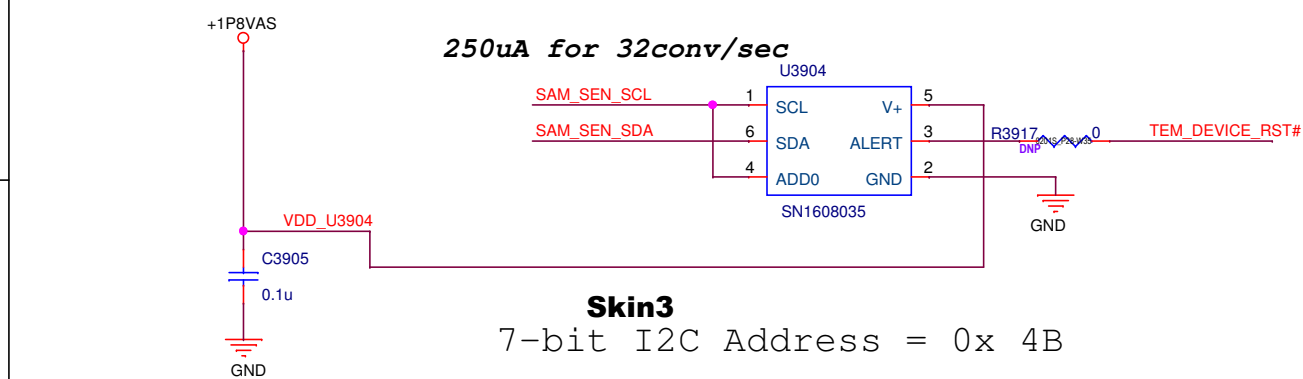
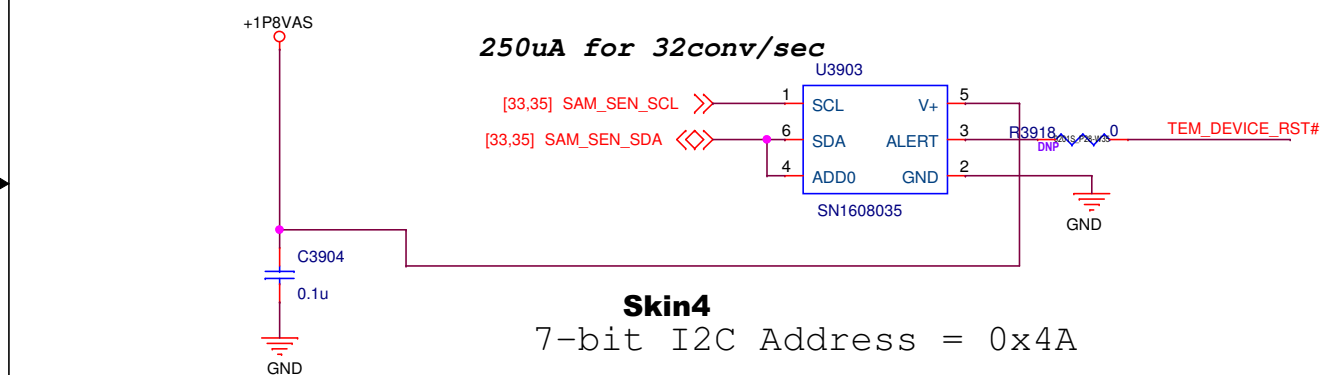
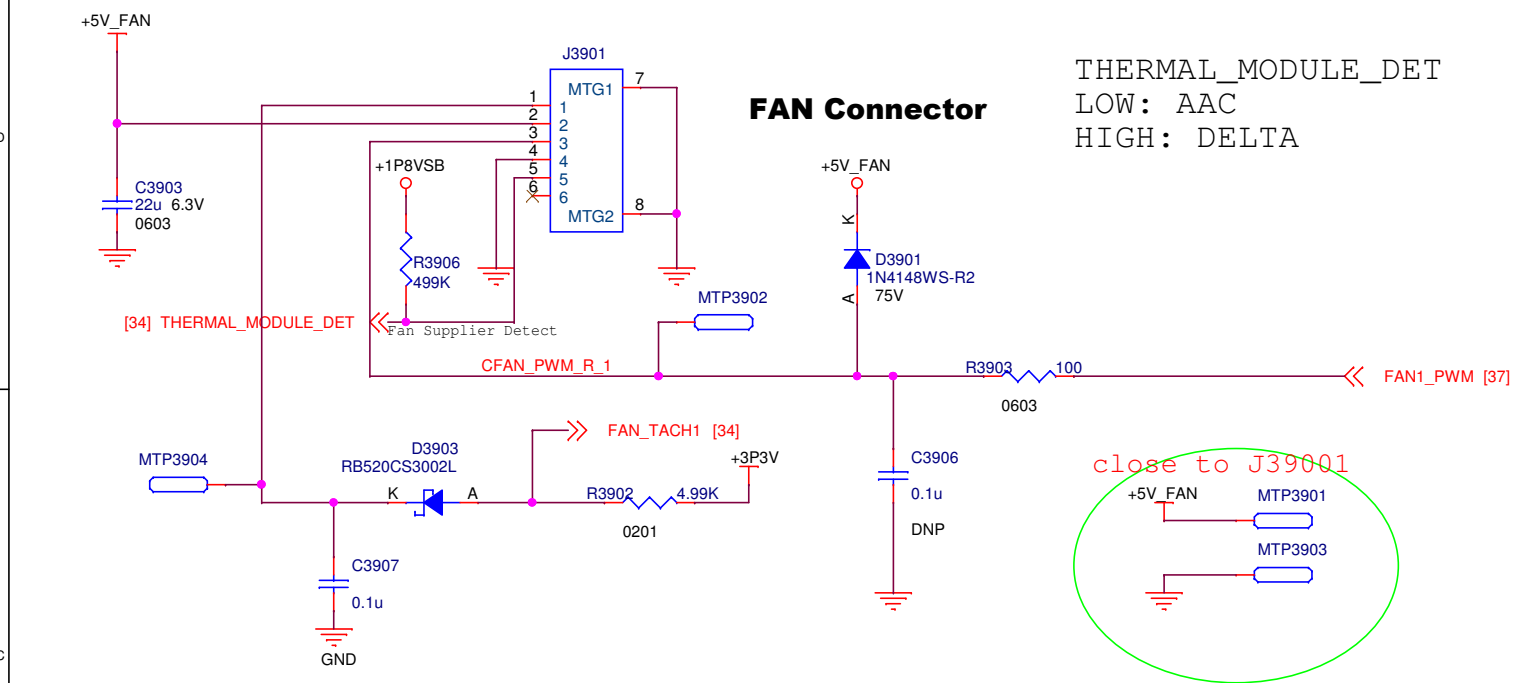
TBL3801

TBL3801		
Ref	Nuvoton	NationZ
R3804	NO-STUFF	X811786-001
R3805	X811786-001	NO-STUFF
R3806	NO-STUFF	X811786-001
R3807	NO-STUFF	X811786-001
R3808	NO-STUFF	X811786-001
R3809	NO-STUFF	X811786-001
C3807	NO-STUFF	M1091281-001
U3801	M1041056-001	M1099468-001



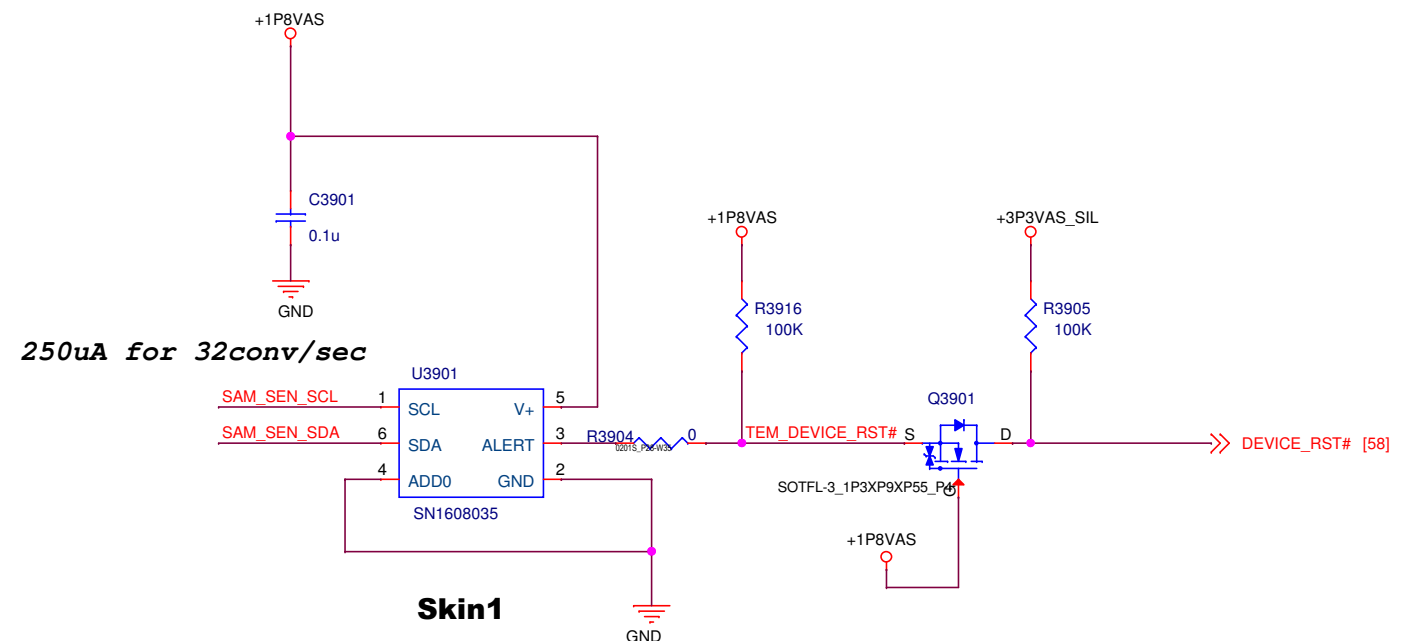
Neet INT Conn, May need add'l cfg for NatZ

+5V_FAN
I_{max}=0.7A
Trace Width>30mil

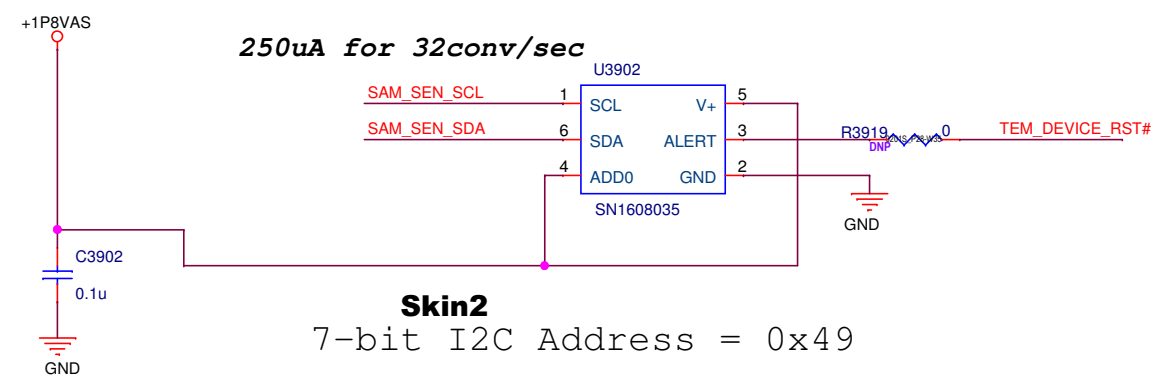


temp sensor for the right location testing

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL



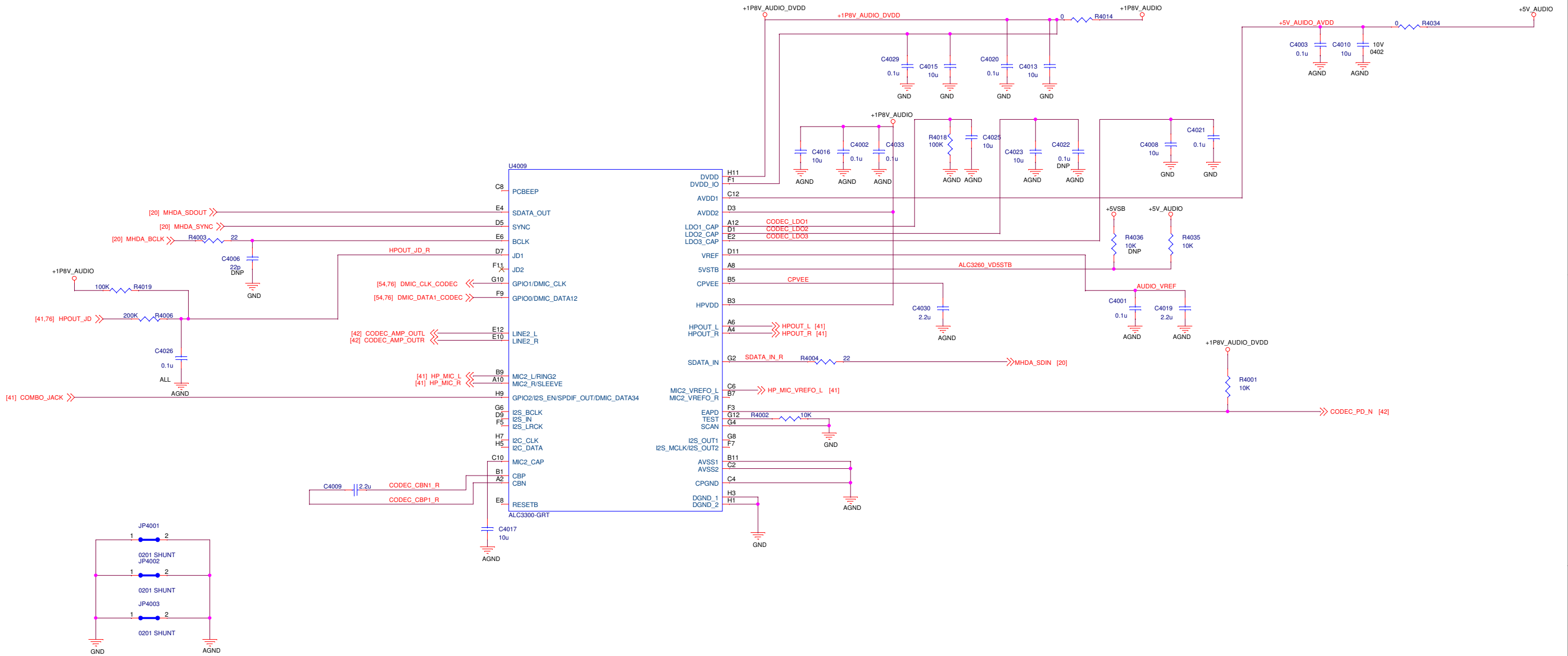
7-bit I2C Address = 0x48



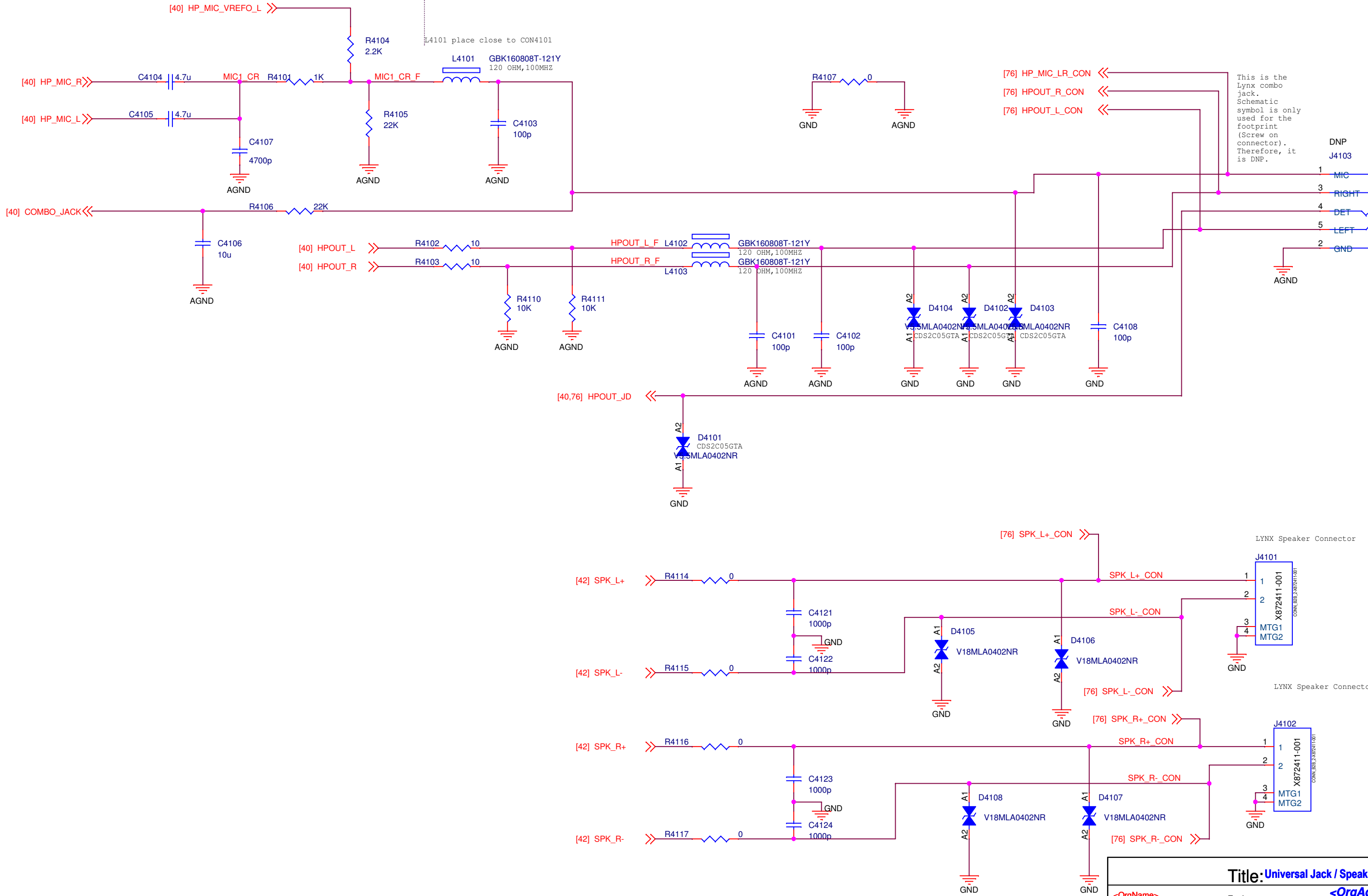
Skin2
7-bit I2C Address = 0x49

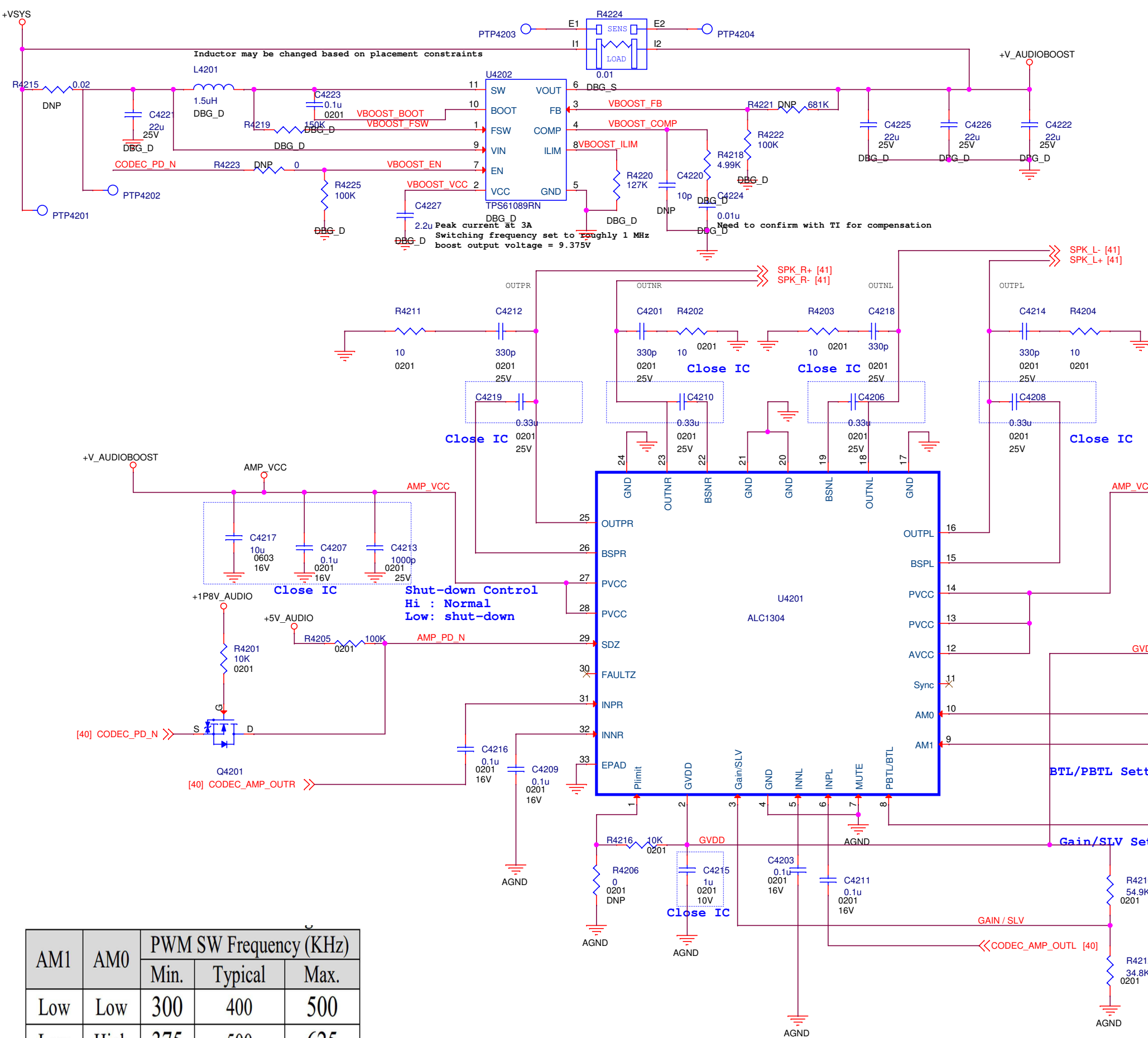
20170908sjs/321
title is: Temp Sensor/ System Fan

Title: Temp Sensor/System Fan	
<OrgName>	Engineer: <OrgAddr1>
Size A3	Project Name EDAN A EV1
Date: Tuesday, May 21, 2019	Rev 1.00
Sheet 39	of 82



HP/MIC1 Combo Jack

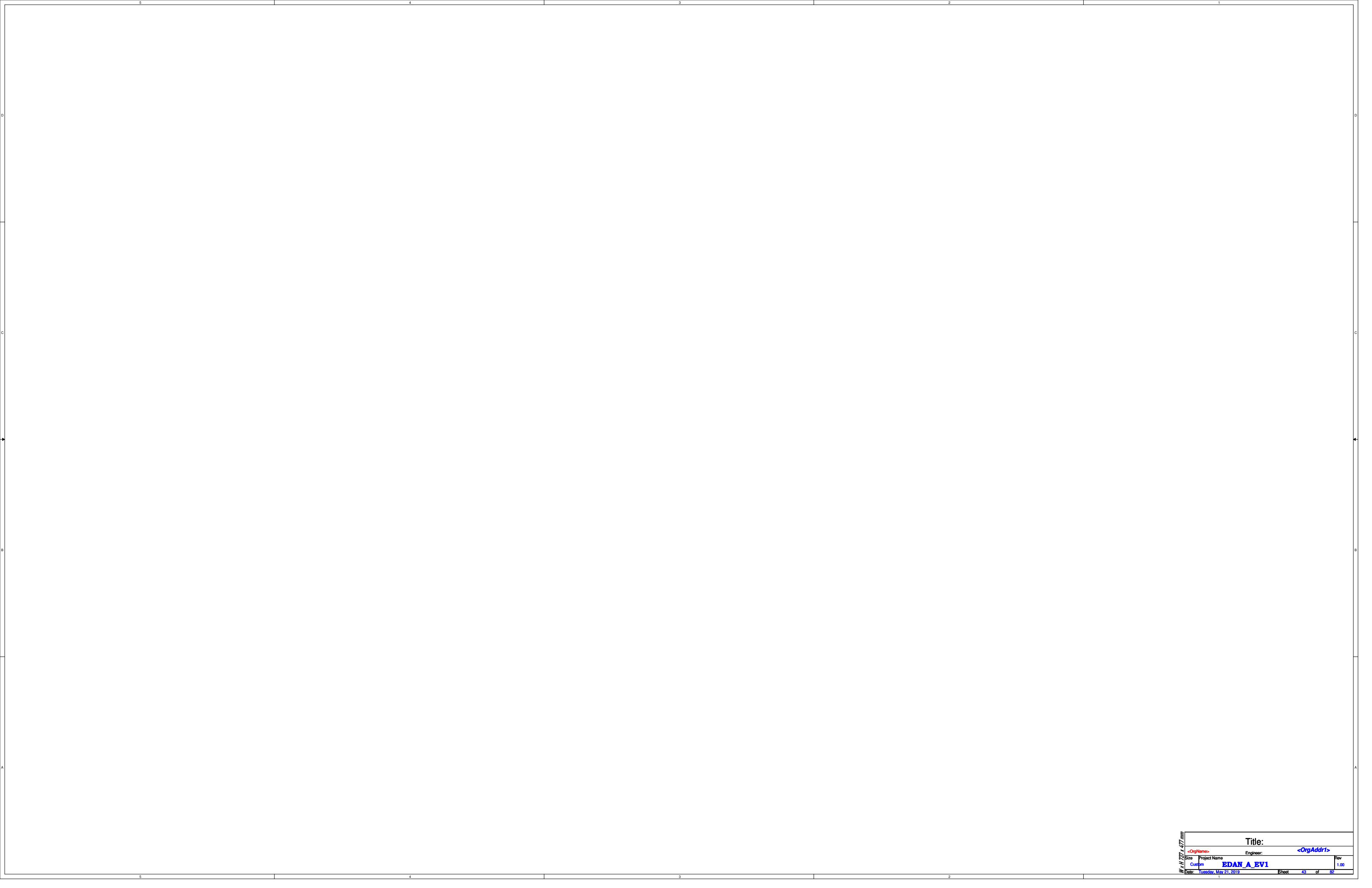


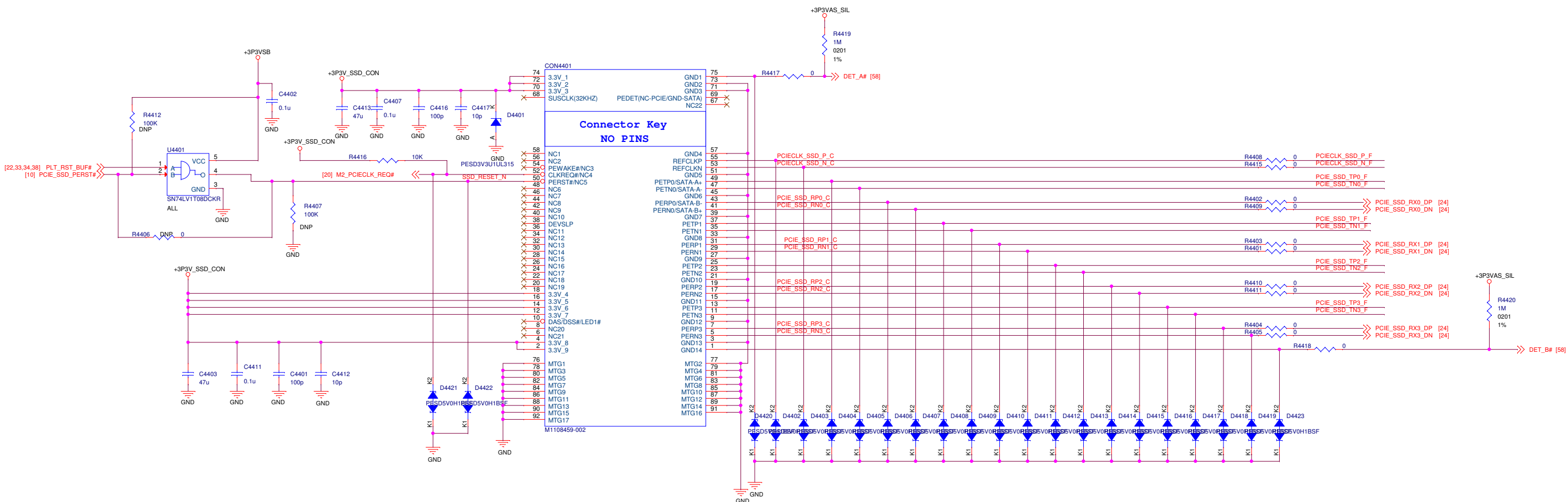
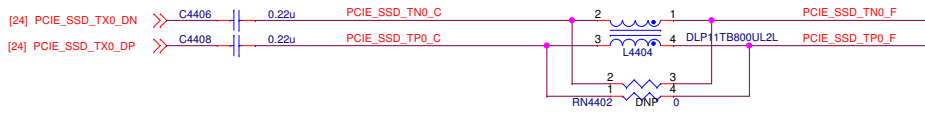
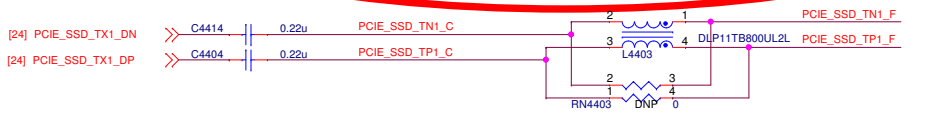
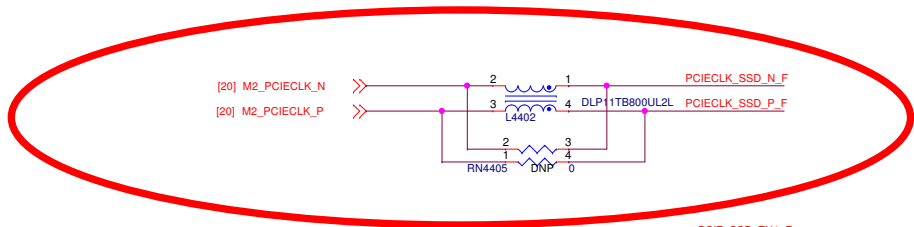


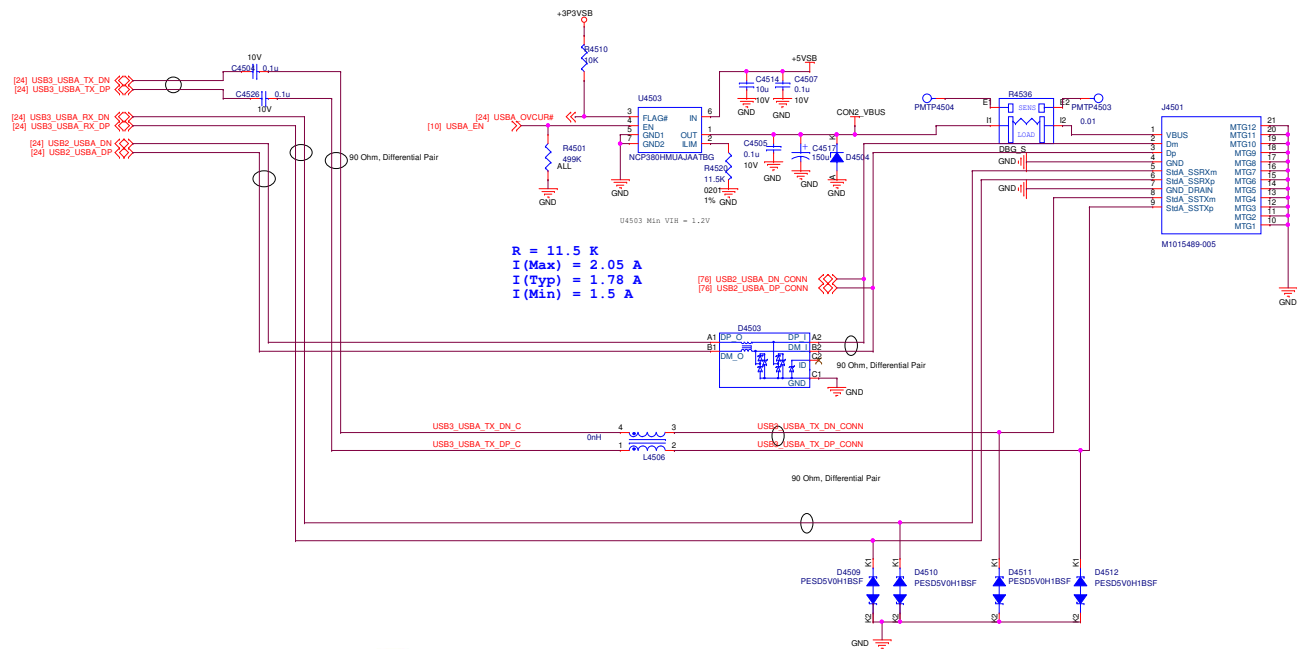
R4210 R4212

Mode	Gain	RX (ohm)	RY (ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	15dB	55K	35K
	20dB	45K	45K
Slave	26dB	35K	55K
	32dB	25K	65K
	15dB	0	NC

AM1	AM0	PWM SW Frequency (KHz)		
		Min.	Typical	Max.
Low	Low	300	400	500
Low	High	375	500	625
High	Low	450	600	750
High	High	750	1000	1250

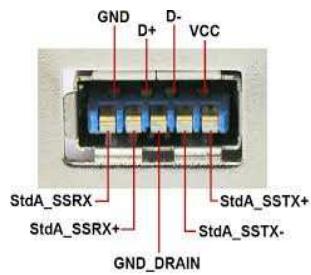


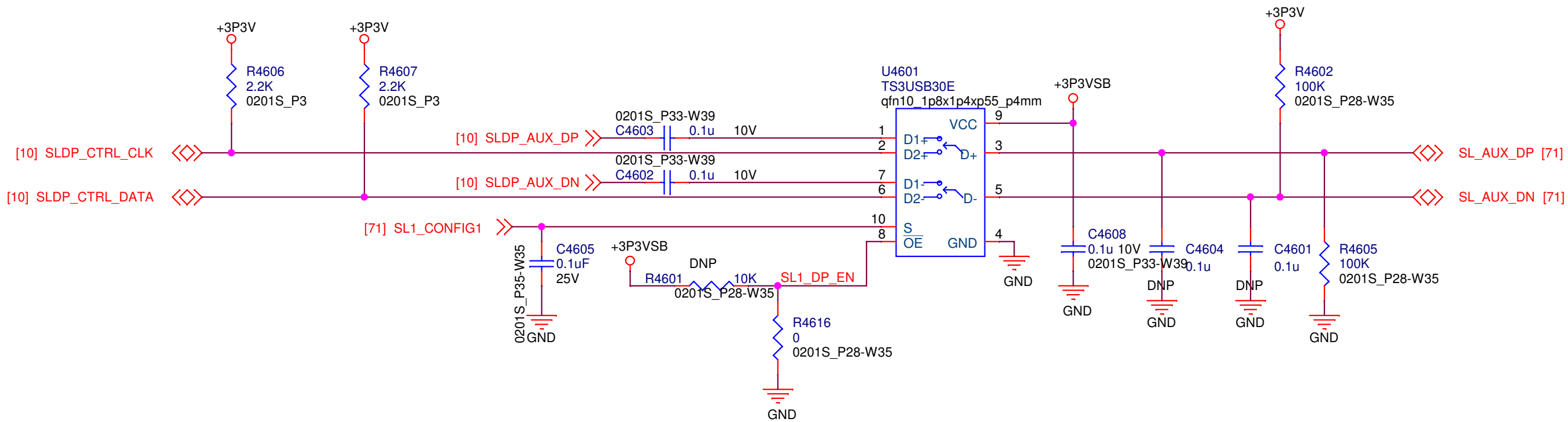




USB 3.0 Connector Pinouts^[44]

Pin	Color	Signal name ("A" Connector)	Signal name ("B" Connector)	Description
Shell	N/A	Shield	Metal housing	
1	Red	VBUS	Power	
2	White	D-	USB 2.0 differential pair	
3	Green	D+		
4	Black	GND	Ground for power return	
5	Blue	StdA_SSRX-	StdB_SSTX-	SuperSpeed transmitter differential pair
6	Yellow	StdA_SSRX+	StdB_SSTX+	
7	N/A	GND_DRAIN	Ground for signal return	
8	Purple	StdA_SSTX-	StdB_SSRX-	SuperSpeed receiver differential pair
9	Orange	StdA_SSTX+	StdB_SSRX+	



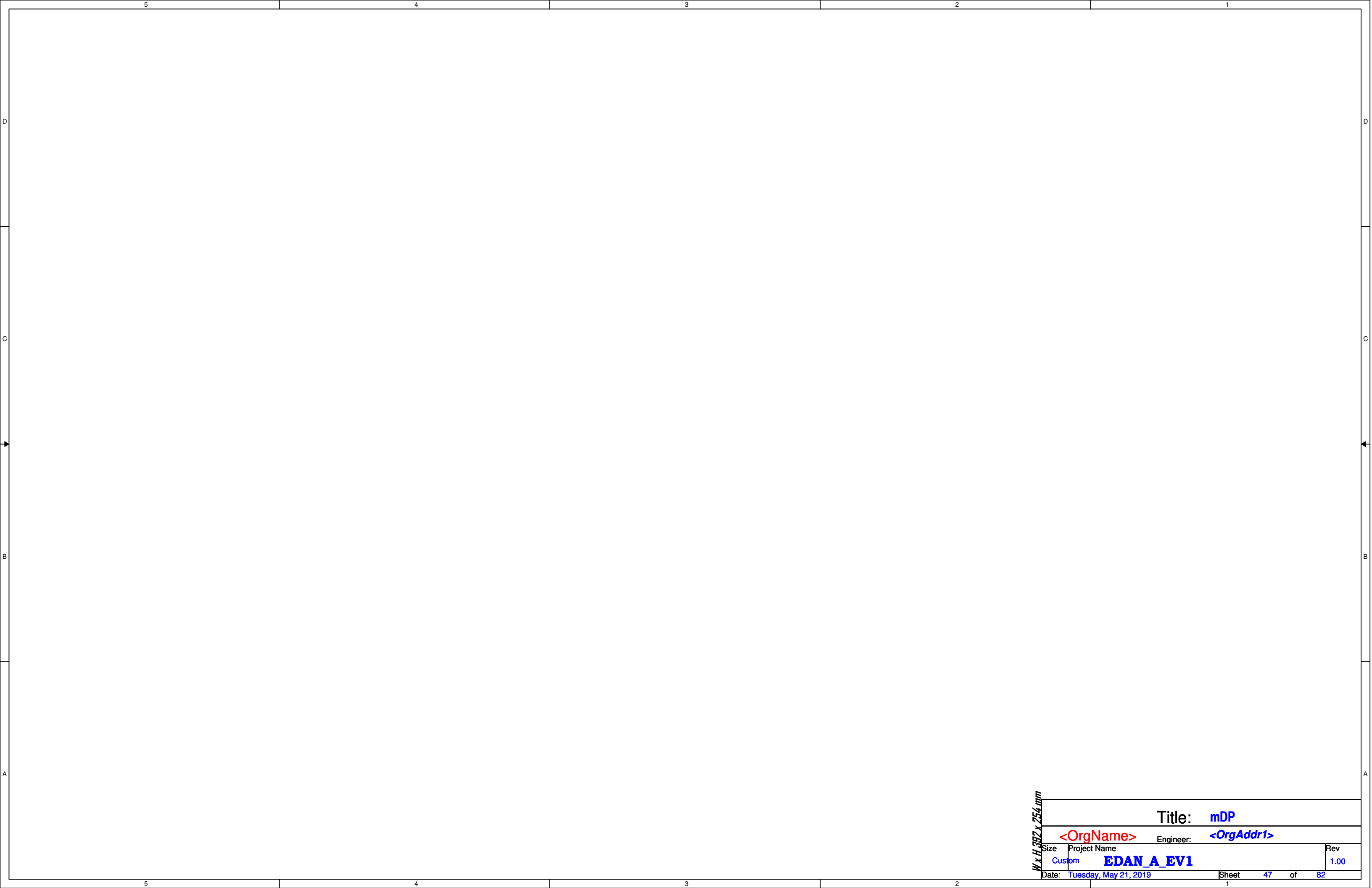


TS3USB30E

EN	S	Connection
L	L	AUX for DP [D1 to D]
L	H	DDC for HDMI [D2 to D]
H	X	HI-Z

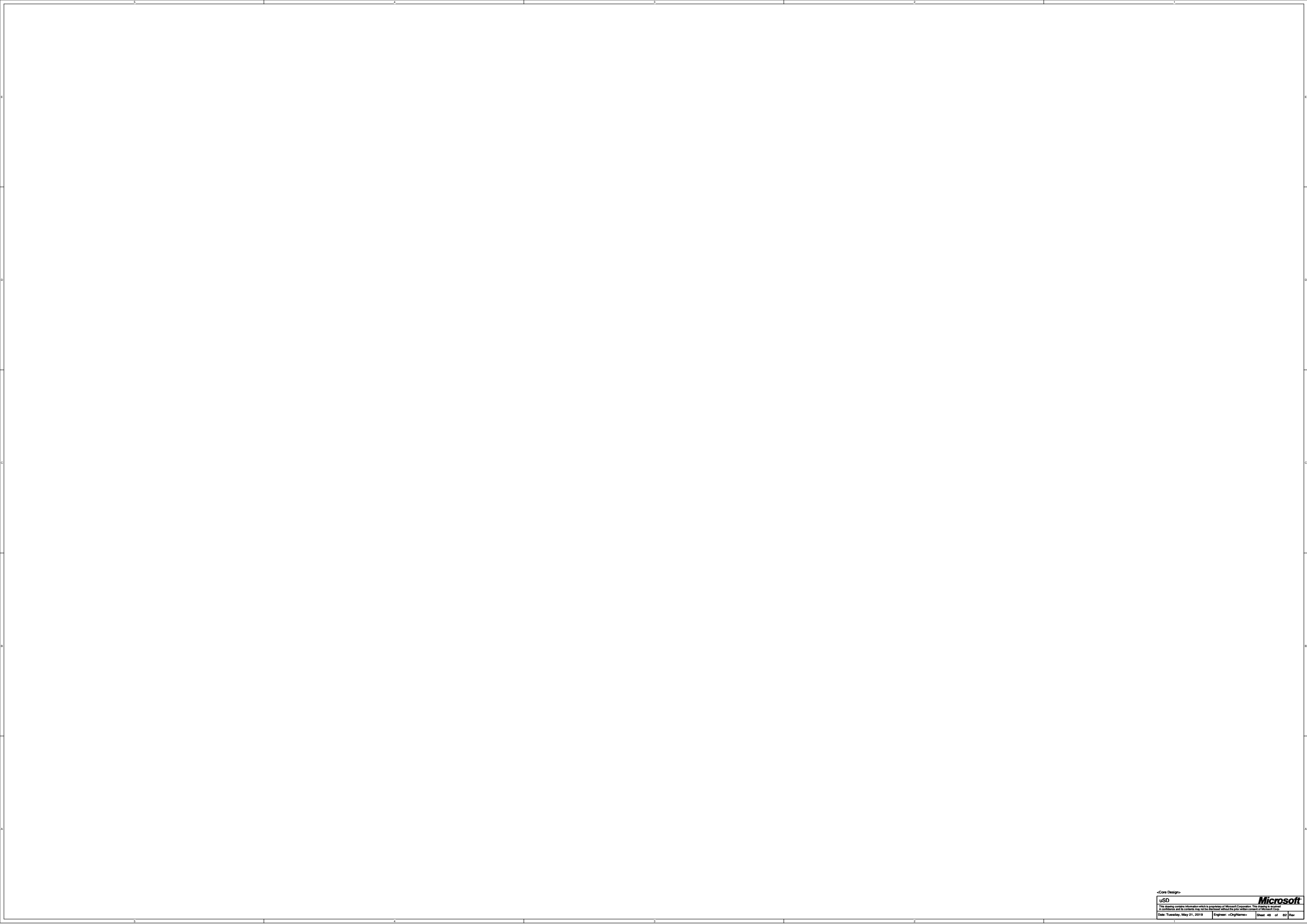
W x H 337 x 218 mm

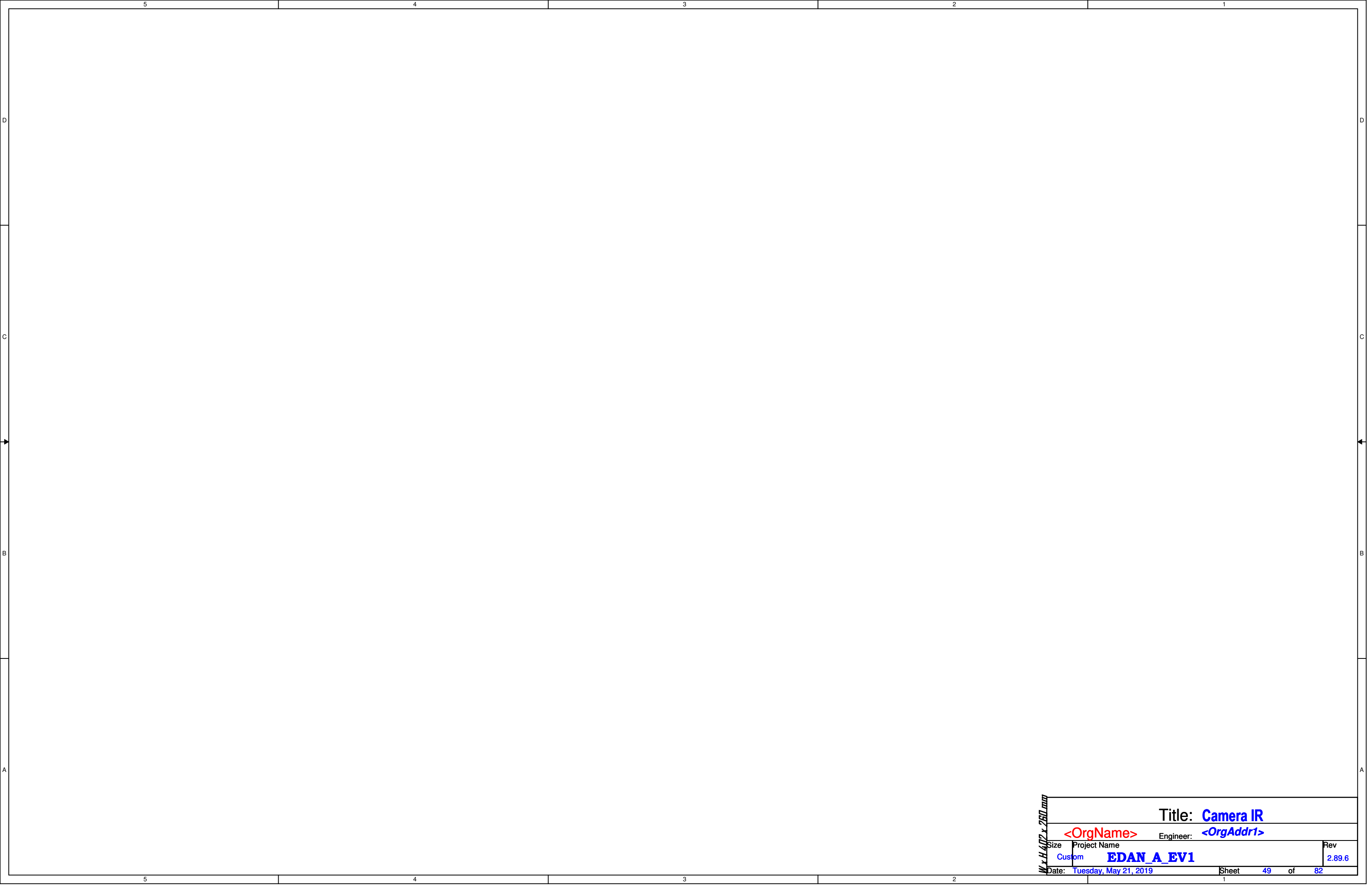
Title: DP Dongle Control		
Engineer: <OrgAddr1>		
Size A4	Project Name EDAN_A_EV1	Rev 1.00
Date: Tuesday, May 21, 2019	Sheet 46	of 82



Title: mDP	
<OrgName>	Engineer: <OrgAddr1>
Size Custom	Project Name EDAN_A_EV1
Date: Tuesday, May 21, 2019	Rev 1.00
Sheet 47 of 82	

W x H 392 x 254 mm





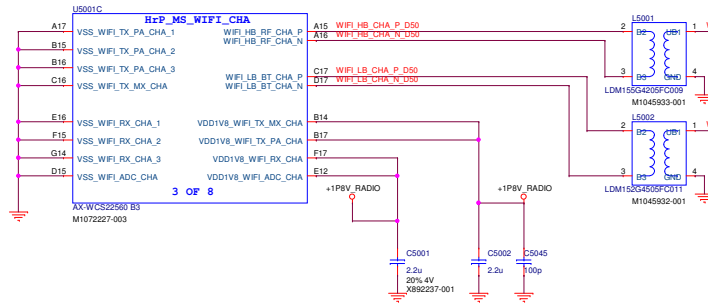
Title: Camera IR			
<OrgName>		Engineer:	<OrgAddr1>
Size	Project Name		Rev
Custom	EDAN_A_EV1		2.89.6
Date:	Tuesday, May 21, 2019		Sheet 49 of 82

W x H 402 x 250 mm

LAYOUT NOTE:
WIFI*D50 and WIFI*S50 routed with impedance control

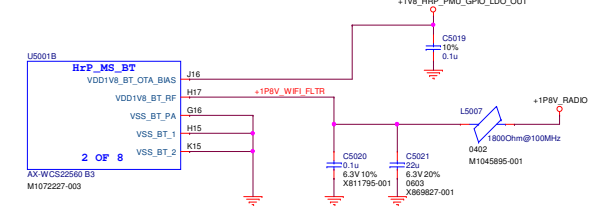
Non-50-Ohm System -> Follow Intel Layout

BT ON CHA LB

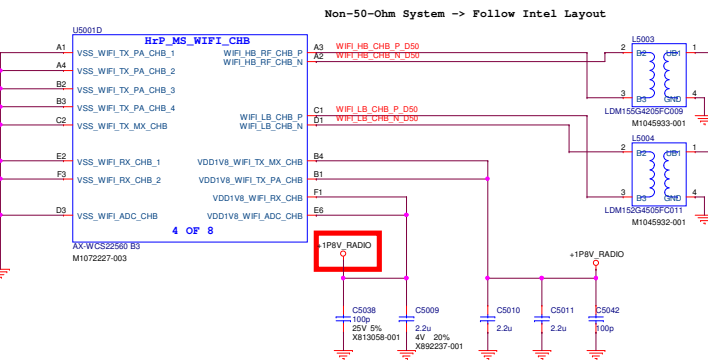
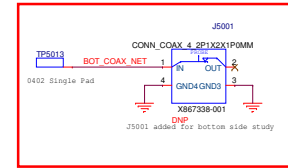


WiFi Harrison Peak

Filters and switches need to be reviewed by RF team and ME



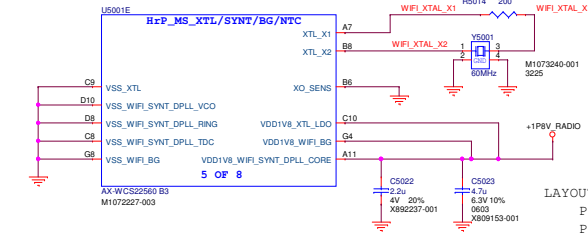
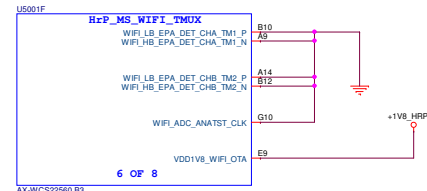
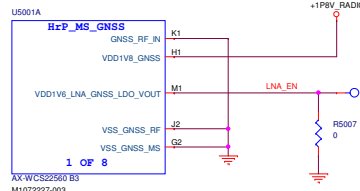
Right antenna connector



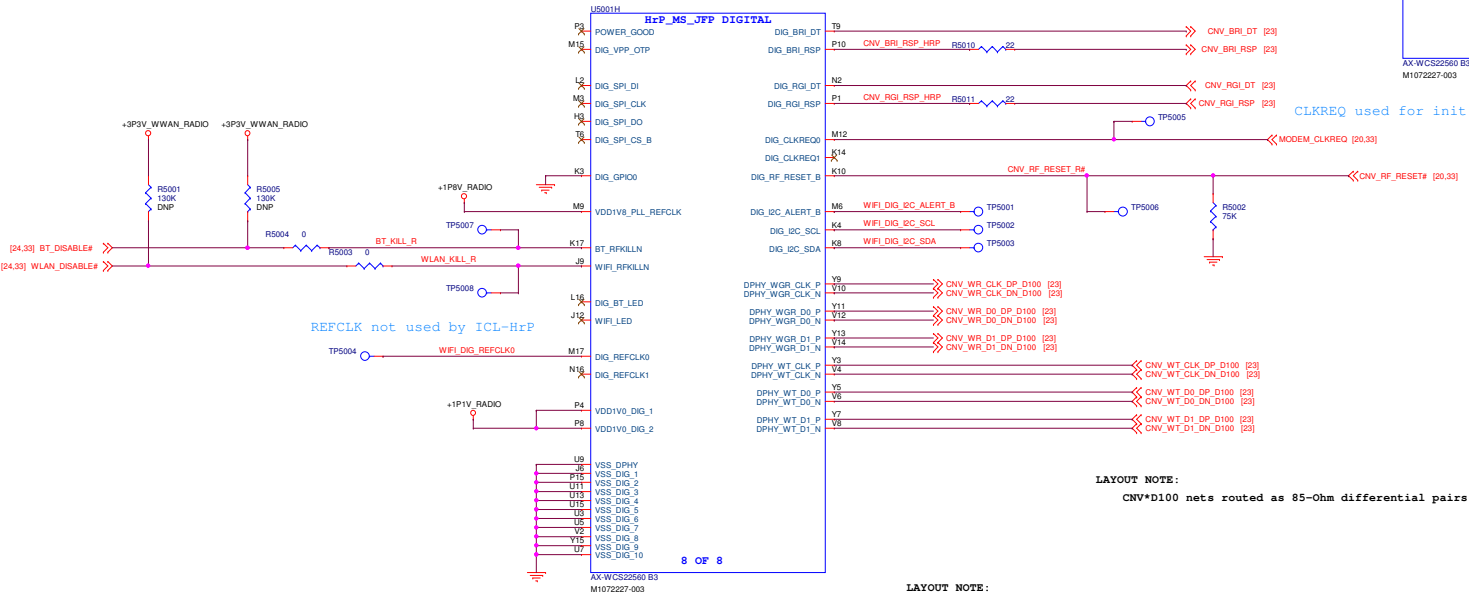
1P8V_RADIO

1P8V_RADIO

Confirm CNV strapping for ICL-HrP only

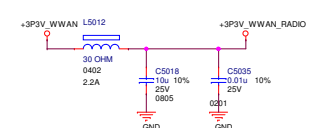


LAYOUT NOTE:
PLACE C5022 at A11
PLACE 4.7UF C5023 as close as possible to A11

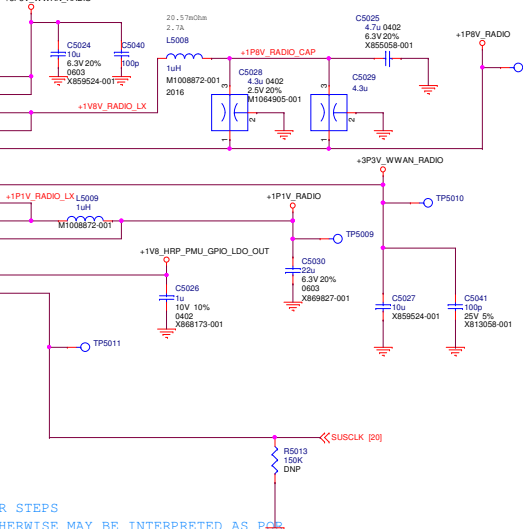


LAYOUT NOTE:
CNV*D100 nets routed as 85-Ohm differential pairs

LAYOUT NOTE:
PLACE CNV_WT* TPS NEAR U5001;
Stubbs should be minimized and limited to just a VIA for access
Consider removing CNV_WT* TPS in later builds



+3P3V_WWAN
3.3V +/- 0.165V
200 mVPP, 10-500kHz
300 mVpp -- allowed power rail noise
TRISE (0-3.3V) < 10mSec
RISING EDGE SHALL BE WITHOUT GLITCHES OR STEPS
RIPPLE SHALL NOT DIP MORE THAN 0.3V; OTHERWISE MAY BE INTERPRETED AS POK





Title: Empty		
Engineer: <OrgAddr1>		
Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00
Date: Tuesday, May 21, 2019	Sheet 51 of 82	1

W x H 377 x 244 mm



Title: Camera power			
<OrgName>		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	EDAN_A_EV1		2.89.6
Date: Tuesday, May 21, 2019	Sheet	52	of 82

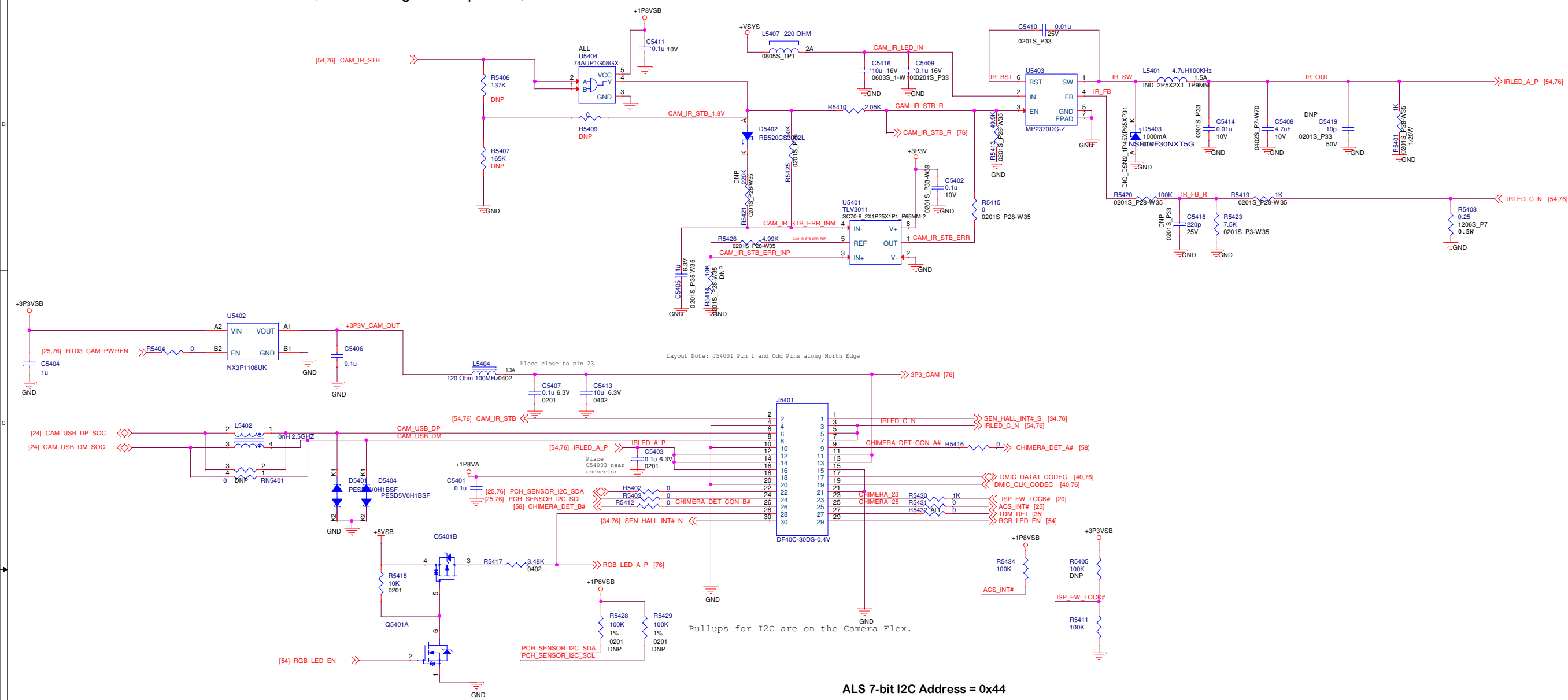
W x H 387 x 250 mm



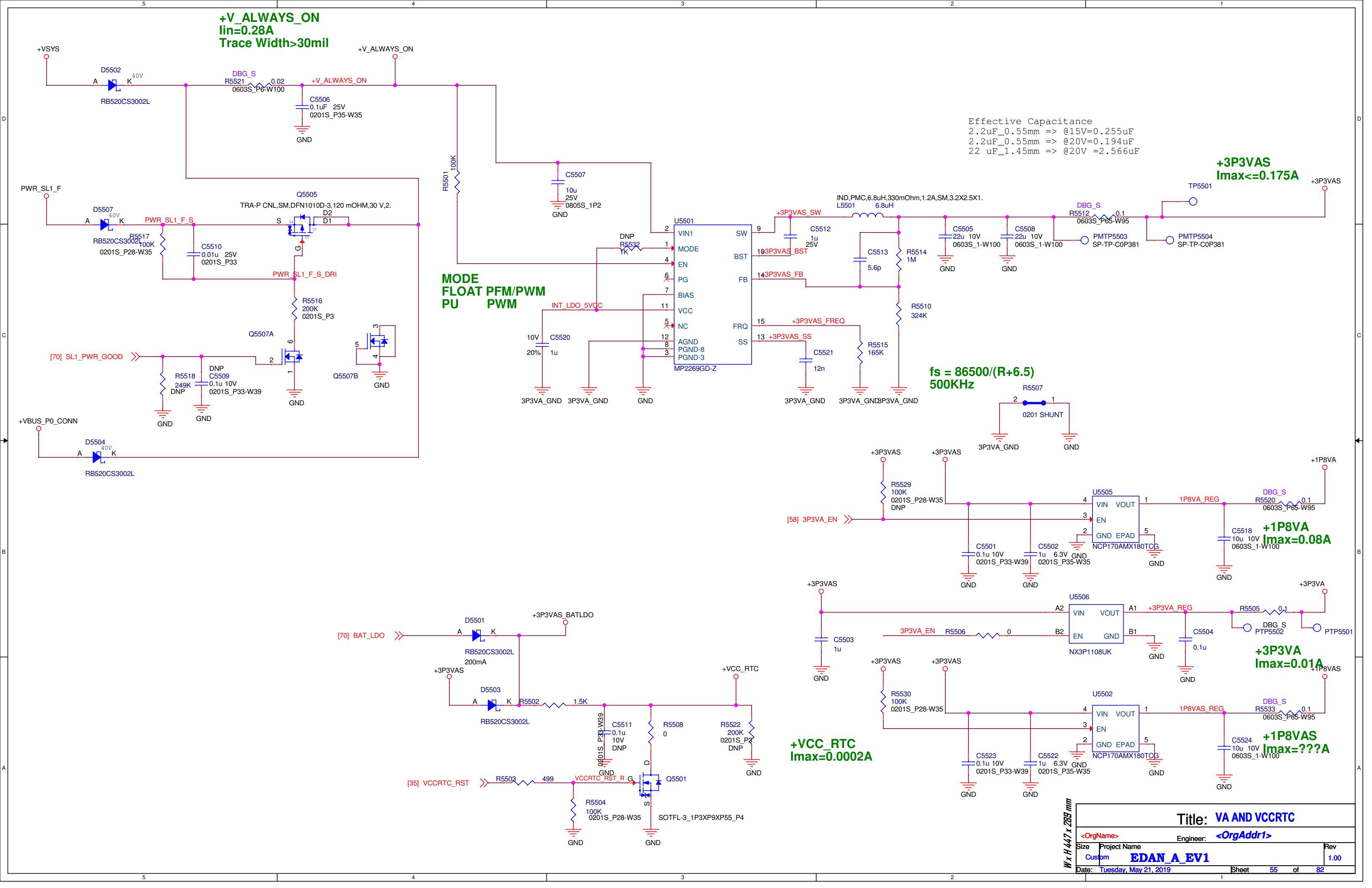
W x H 437 x 328 mm

Title: Blank			
<OrgName>		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	EDAN_A_EV1		2.89.6
Date:	Tuesday, May 21, 2019	Sheet	53 of 82

Sensor Connector to IR and RGB Cameras, Left and Right Microphones, and ALS Sensor



Check with Camera/RF/Power team for regulation, filtering, and component info
Power regulation, Privacy LED and sensors moved locally on
sensor board. IRLED Buck regulation local to mb
Odd side of the J54001 connector faces the North edge of the PCB



+V_ALWAYS_ON
lin=0.28A
Trace Width>30mil

Effective Capacitance
2.2uF_0.55mm => @15V=0.255uF
2.2uF_0.55mm => @20V=0.194uF
22 uF_1.45mm => @20V =2.566uF

+3P3VAS
I_{max}≤0.175A

f_s = 86500/(R+6.5)
500KHz

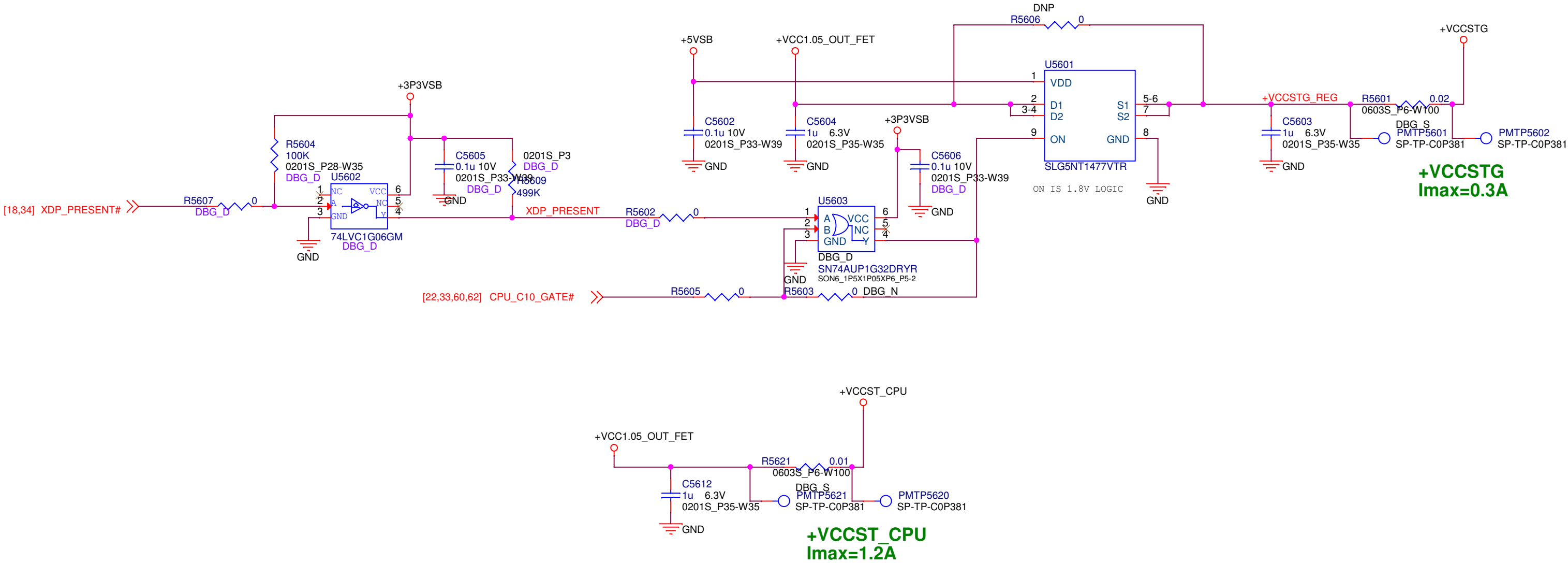
+1P8VA
I_{max}=0.08A

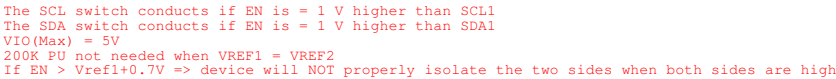
+3P3VA
I_{max}=0.01A

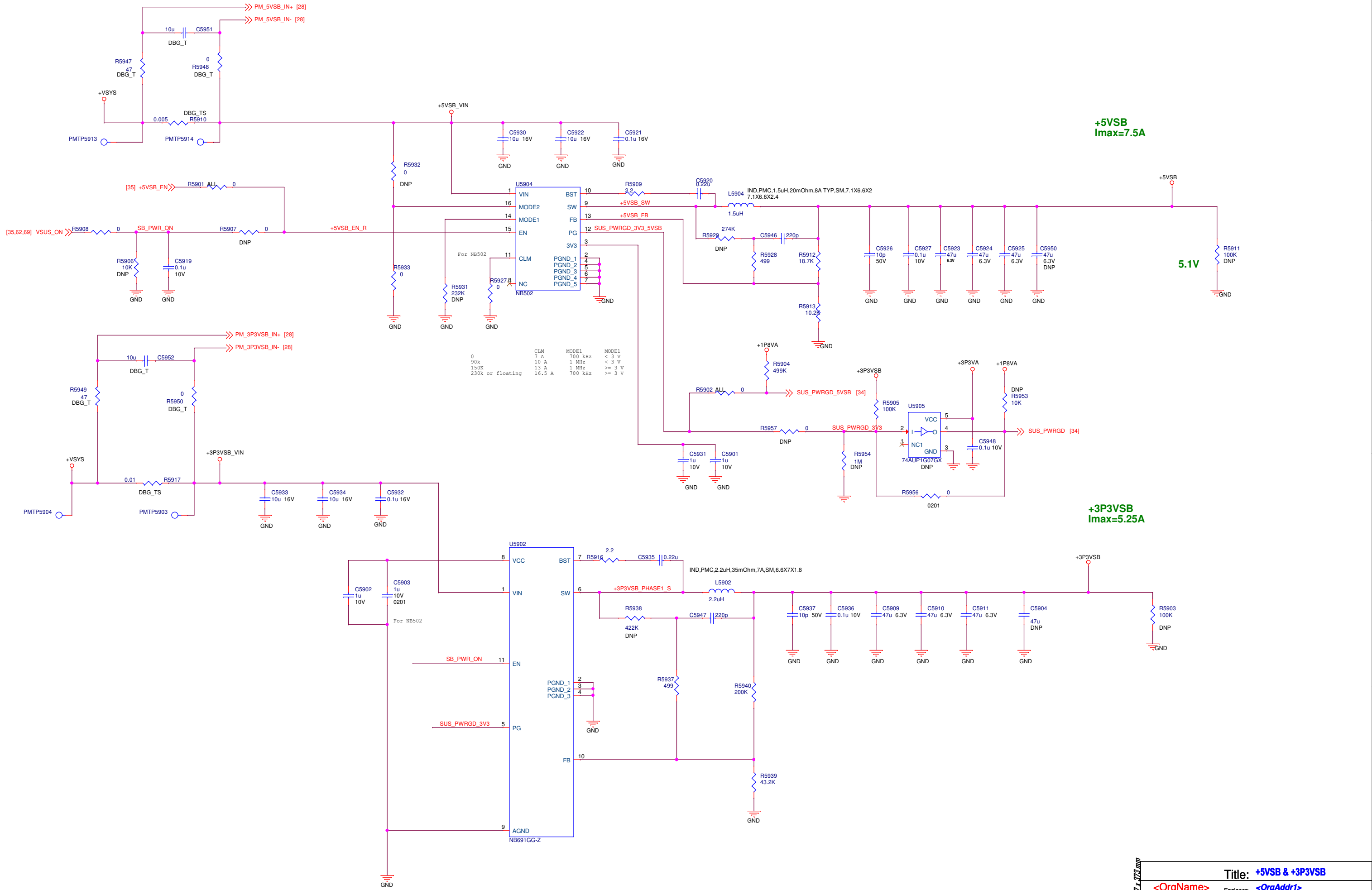
+1P8VAS
I_{max}=???A

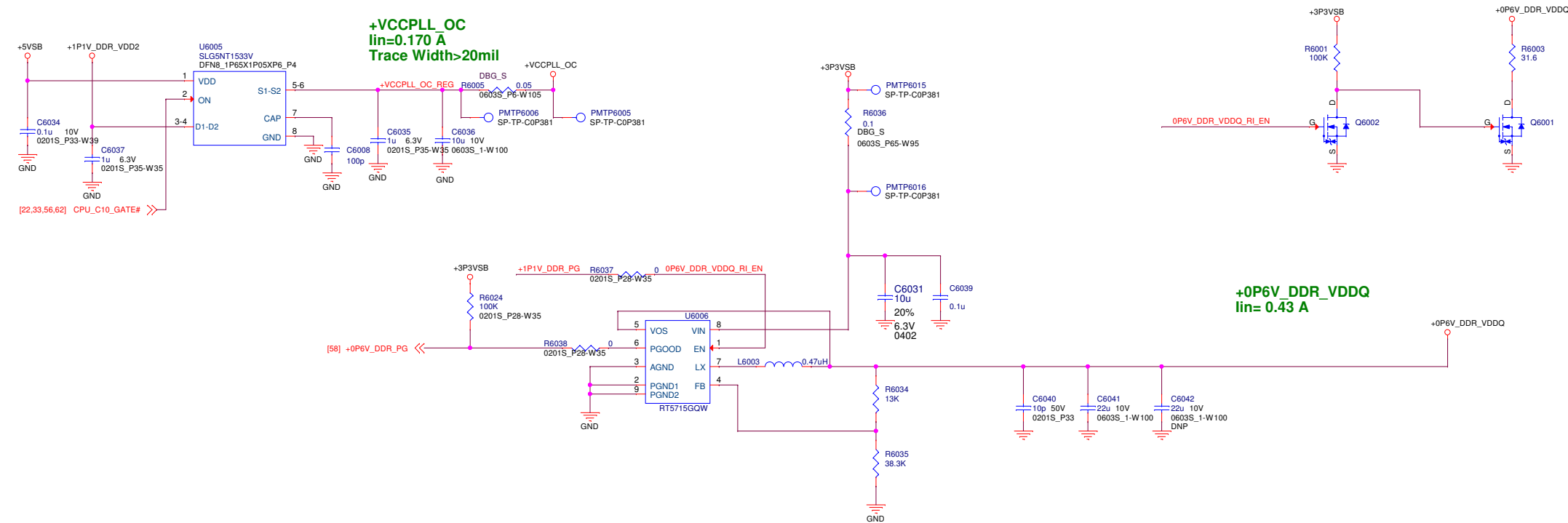
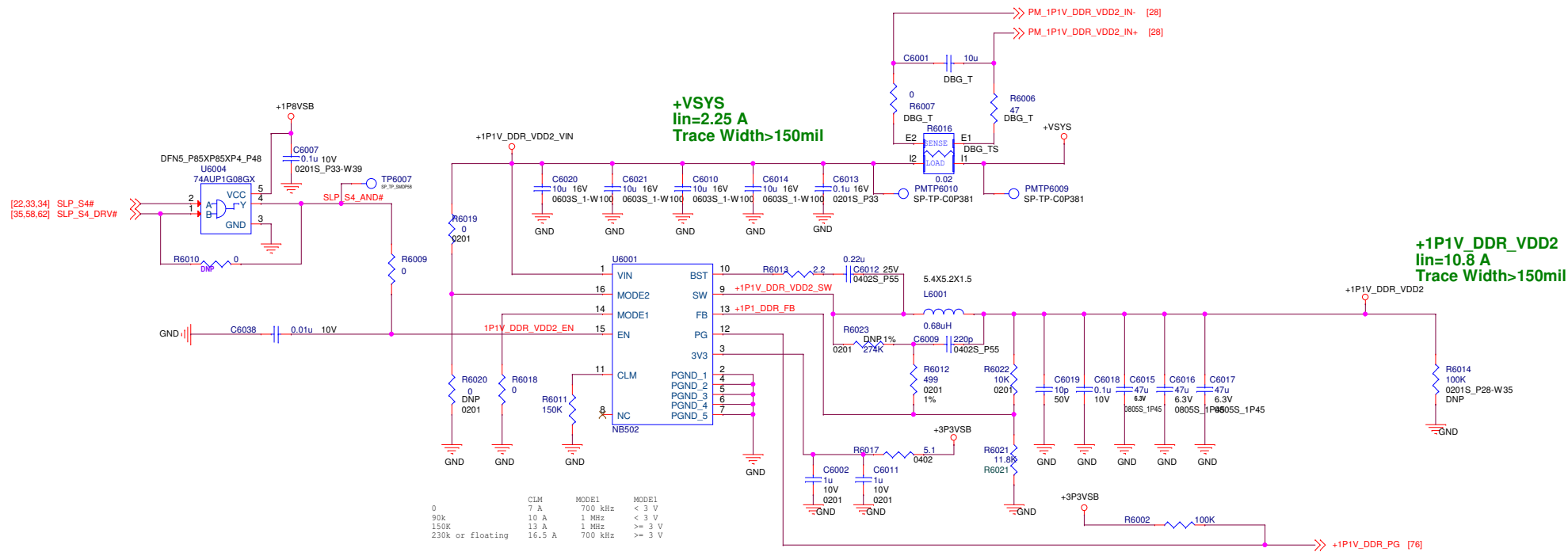
+VCC_RTC
I_{max}=0.0002A

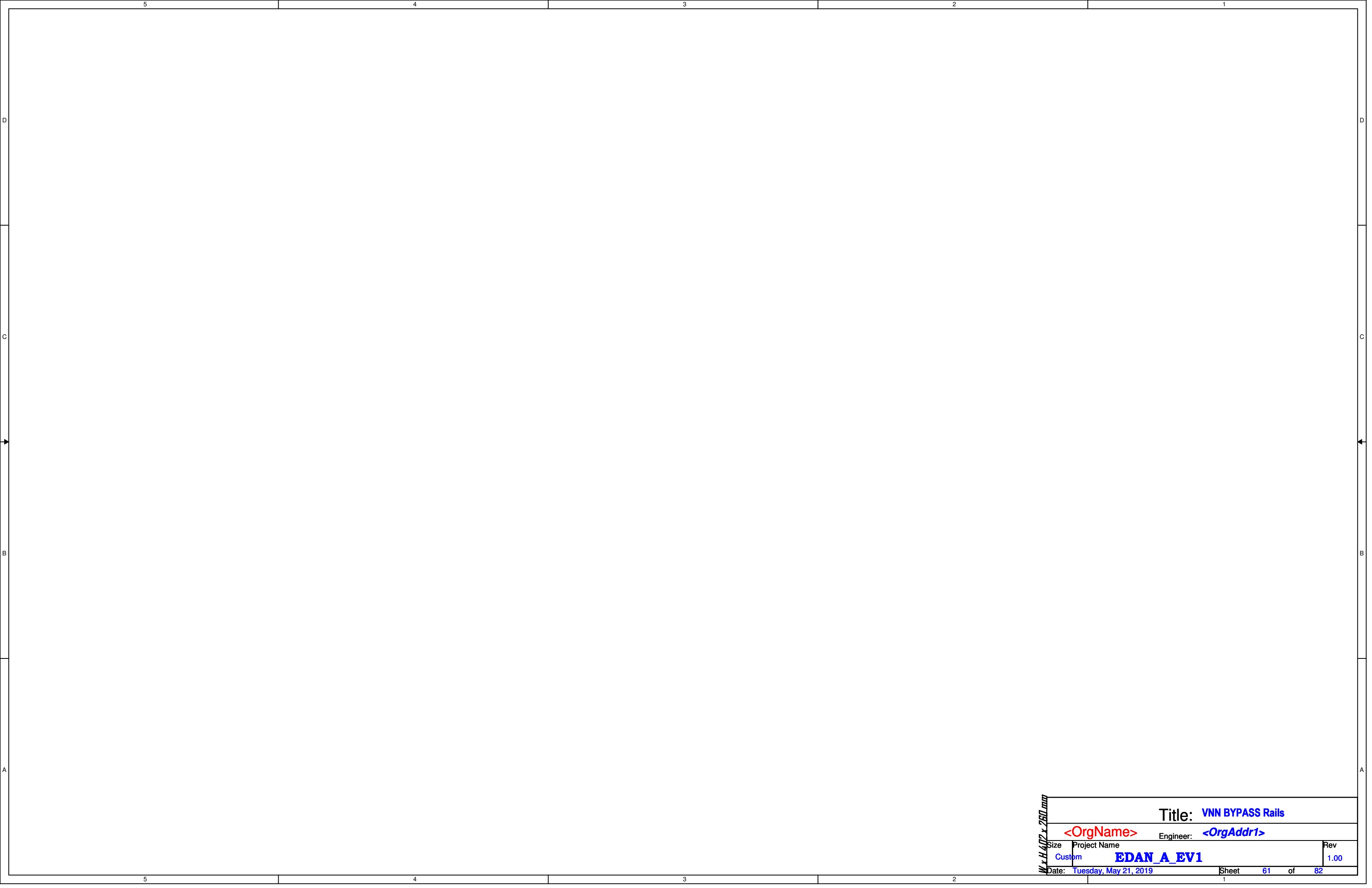
Title: VA AND VCCRTC			
<OrgName>		Engineer: <OrgAddr1>	
Size	Project Name	Rev	1.00
Custom	EDAN_A_EV1		
Date: Tuesday, May 21, 2019		Sheet	55 of 82





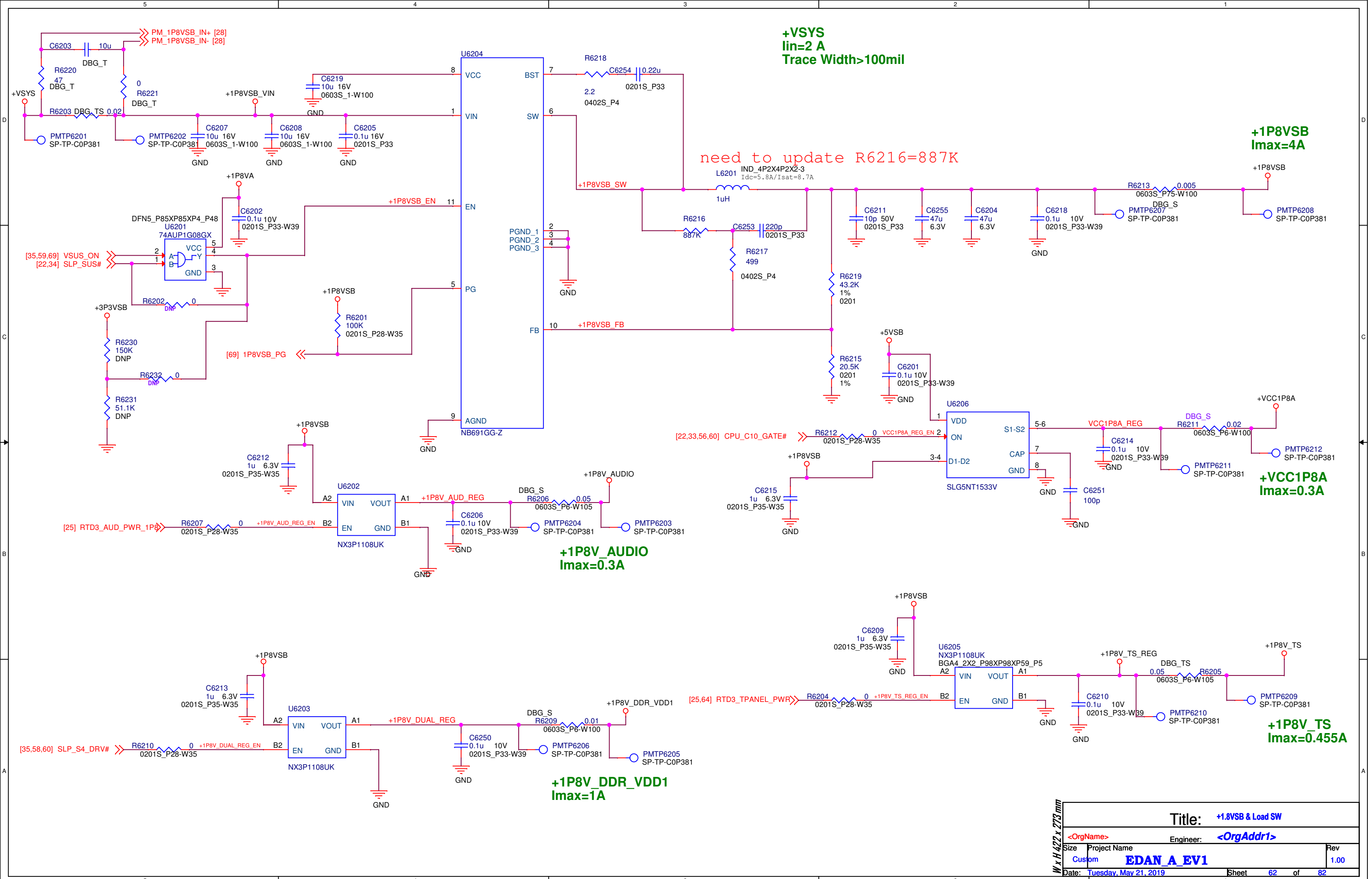


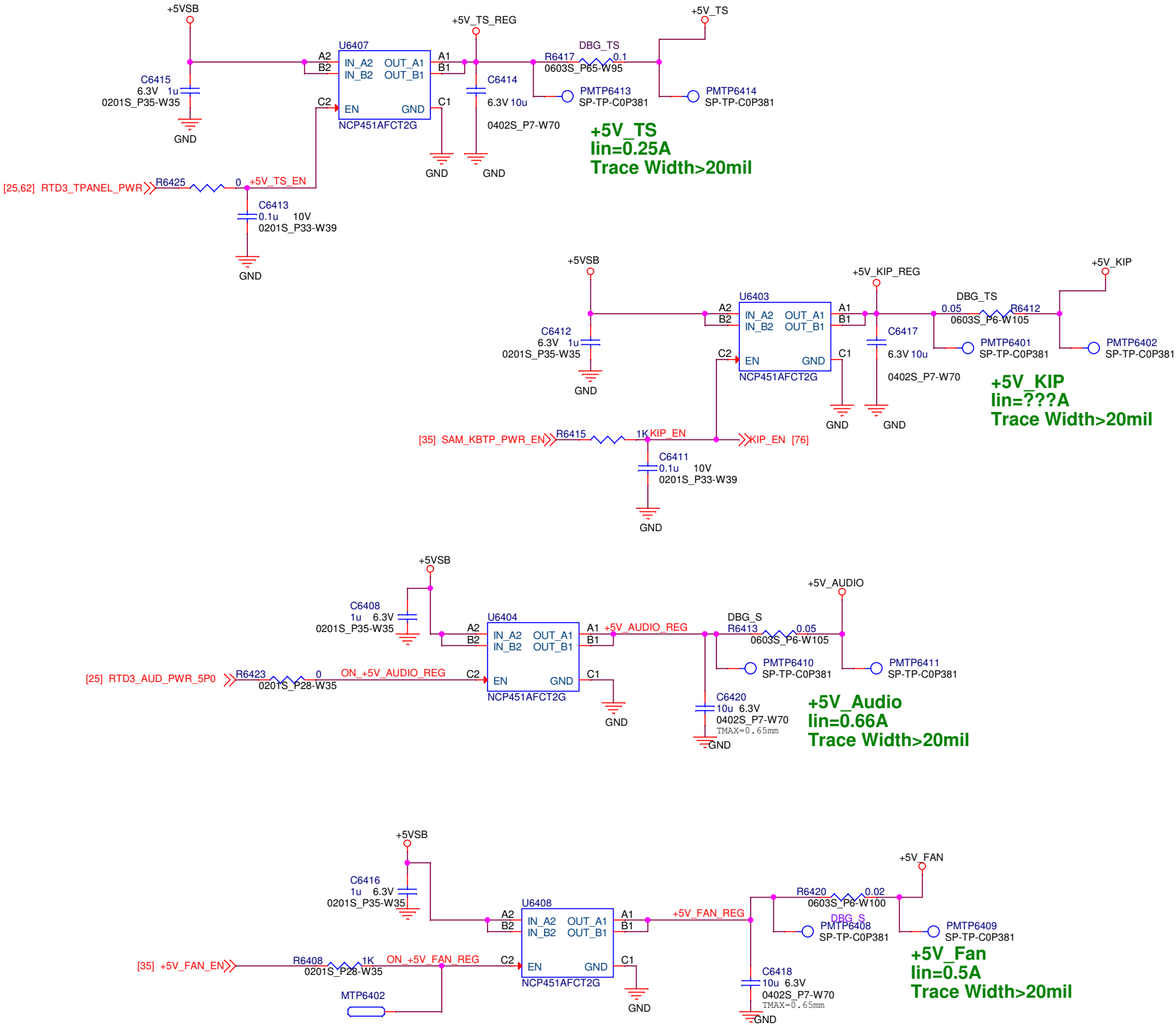




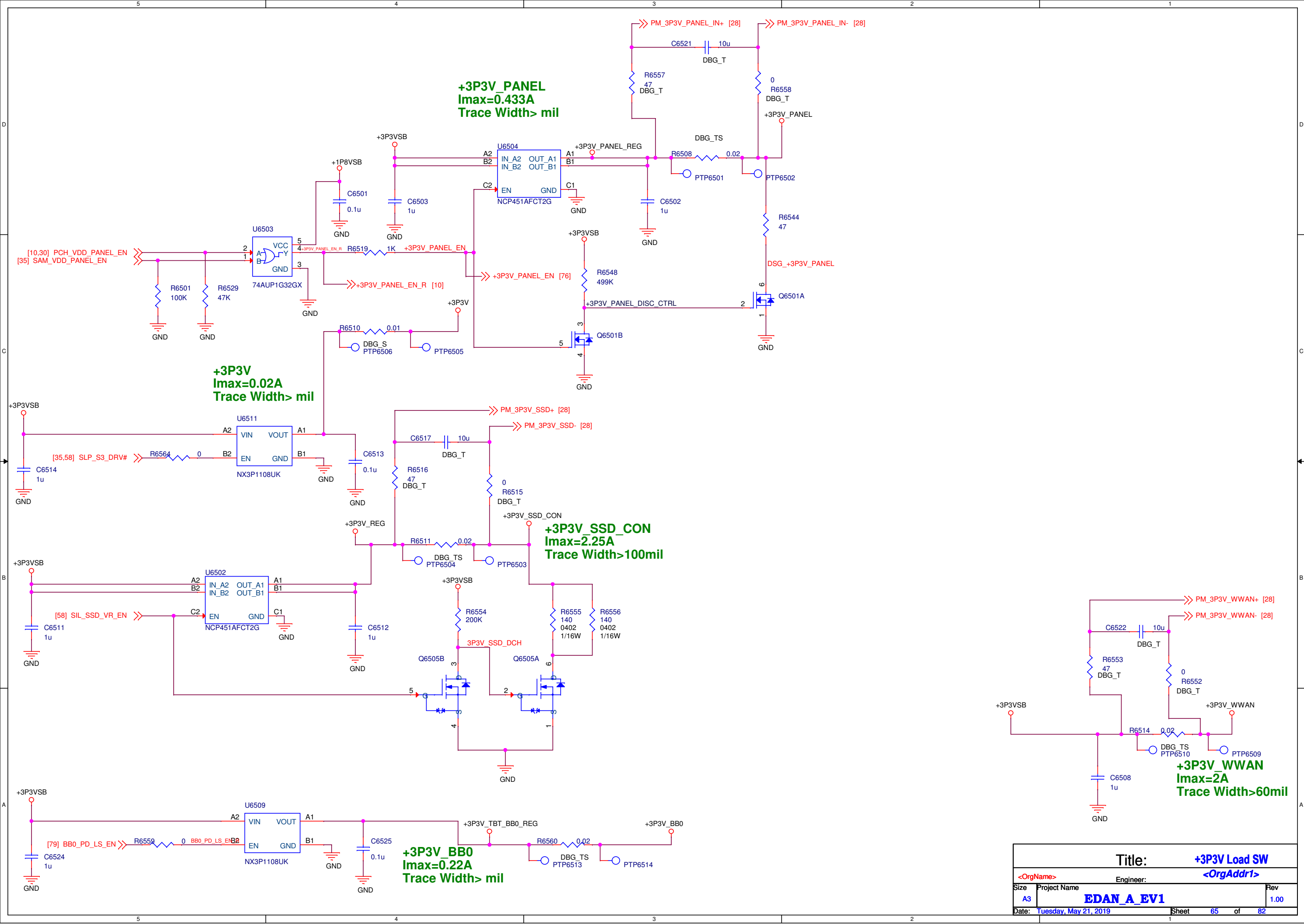
Title: VNN BYPASS Rails			
<OrgName>		Engineer: <OrgAddr1>	
Size Custom	Project Name EDAN_A_EV1	Rev 1.00	
Date: Tuesday, May 21, 2019	Sheet 61 of 82	1	

W x H 402 x 250 mm

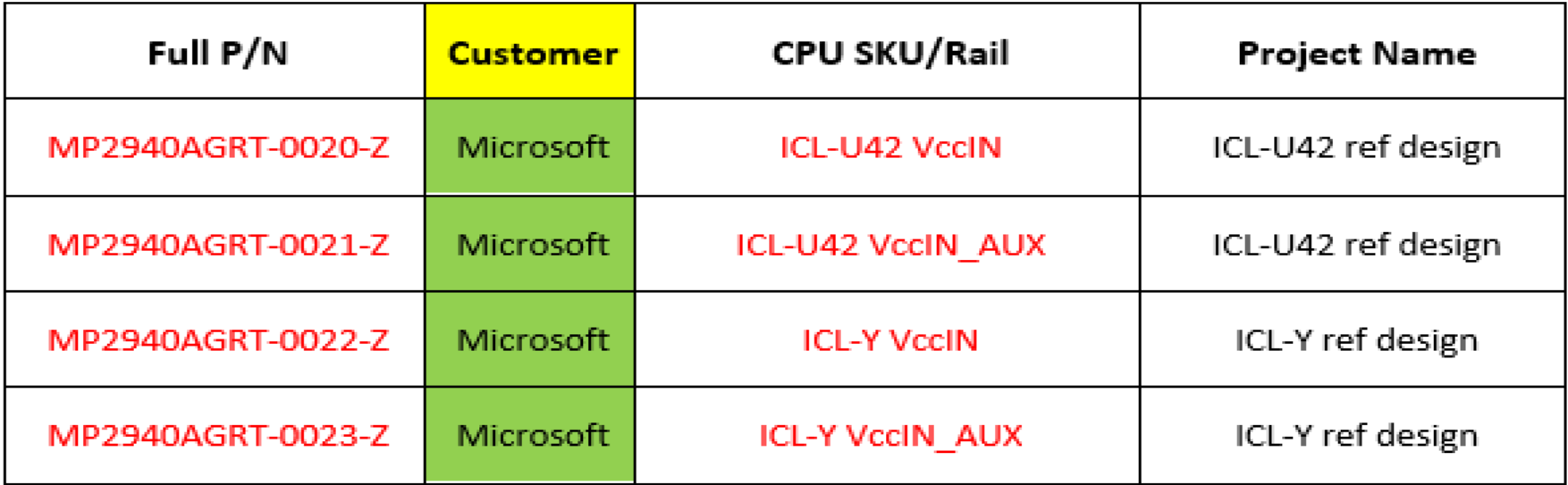


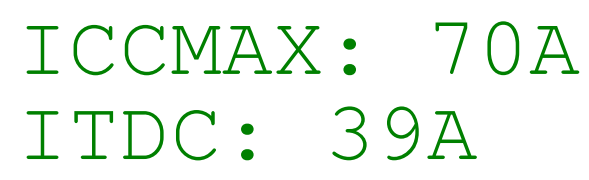


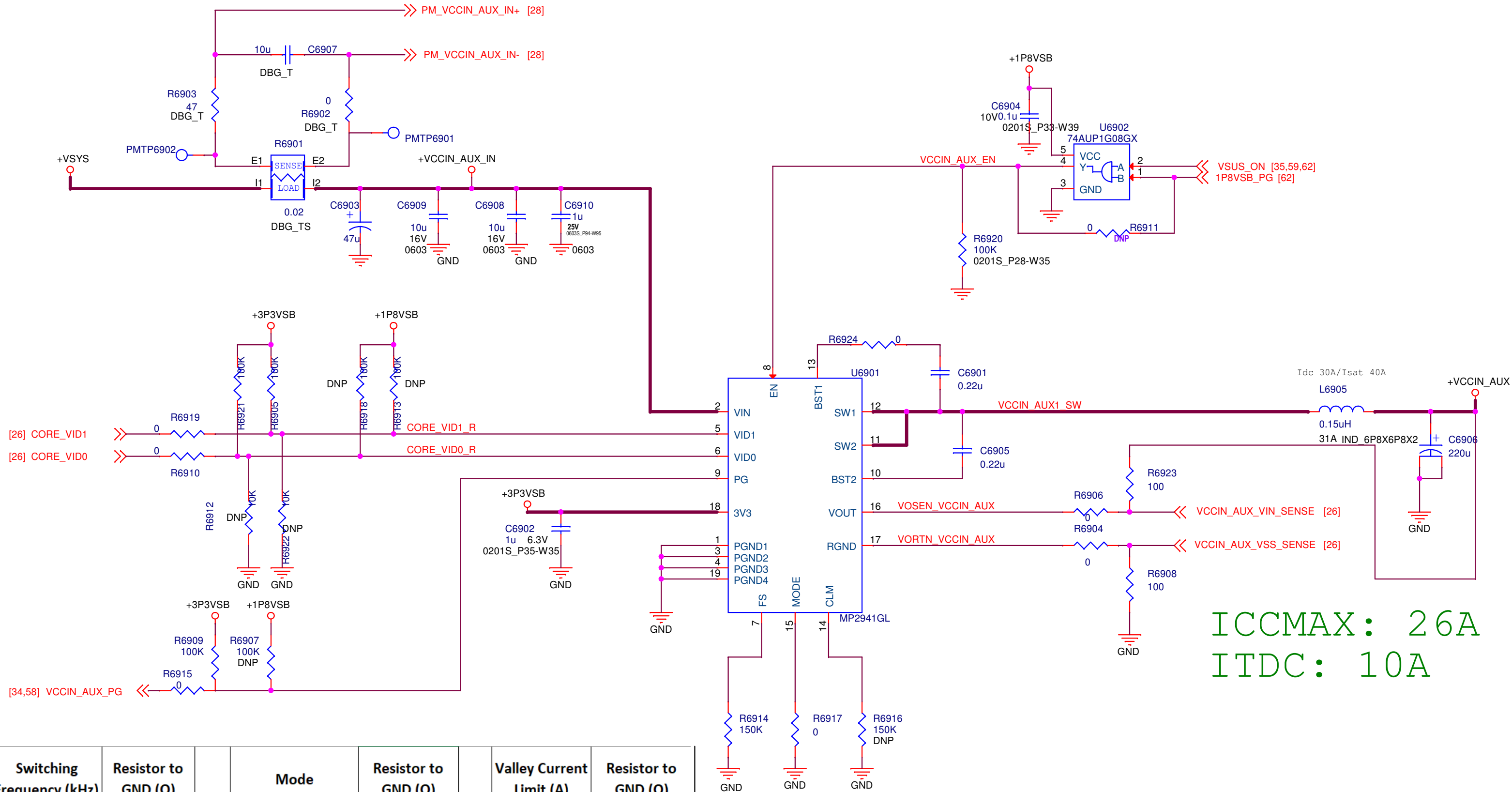
Title: +5V Load SW		
Engineer: <OrgAddr1>		
Size A3	Project Name EDAN_A_EV1	Rev 1.00
Date: Tuesday, May 21, 2019	Sheet 64	of 82



Title: +3P3V Load SW		
Engineer: <OrgAddr1>		
Size A3	Project Name EDAN_A_EV1	Rev 1.00
Date: Tuesday, May 21, 2019	Sheet 65	of 82

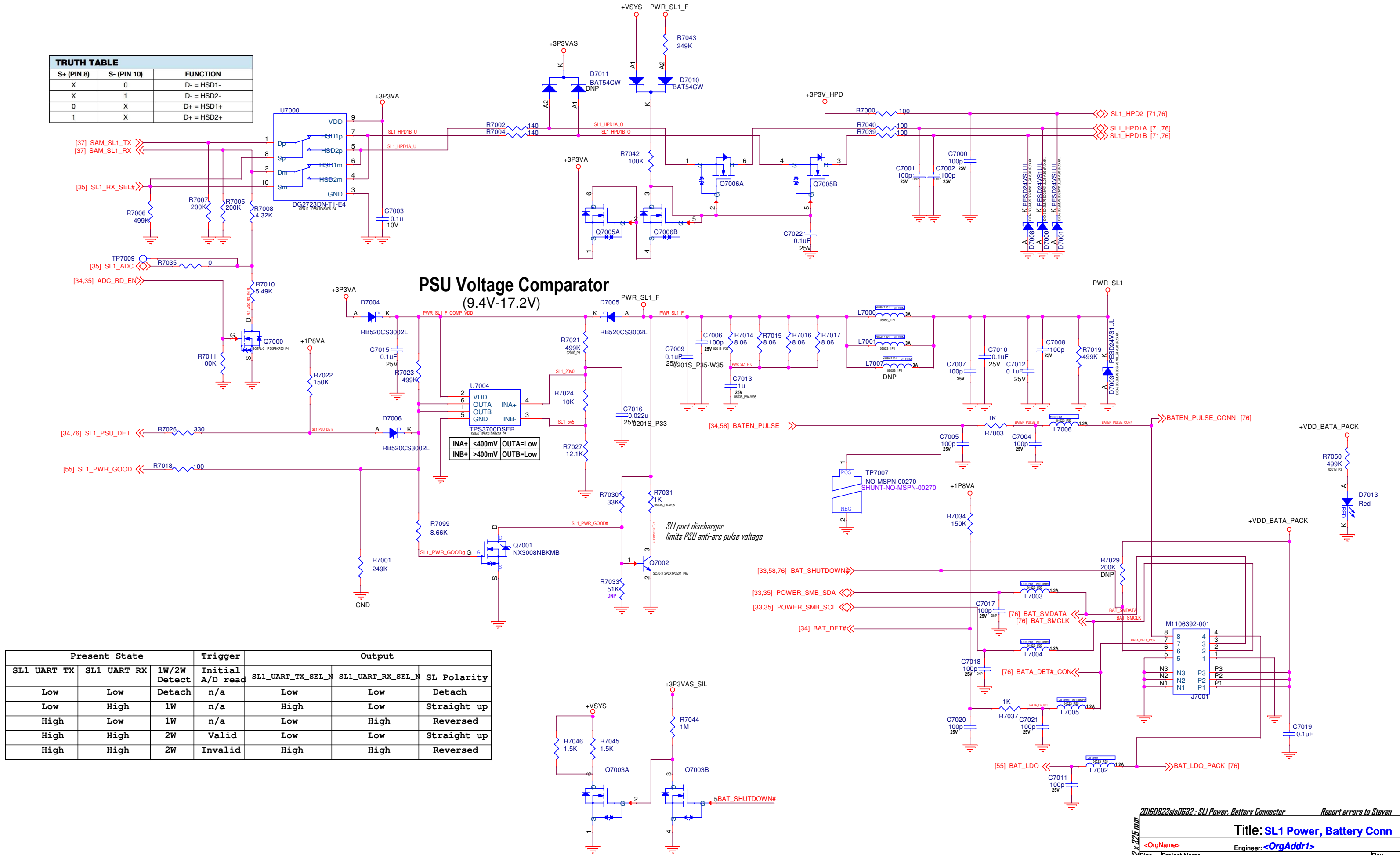




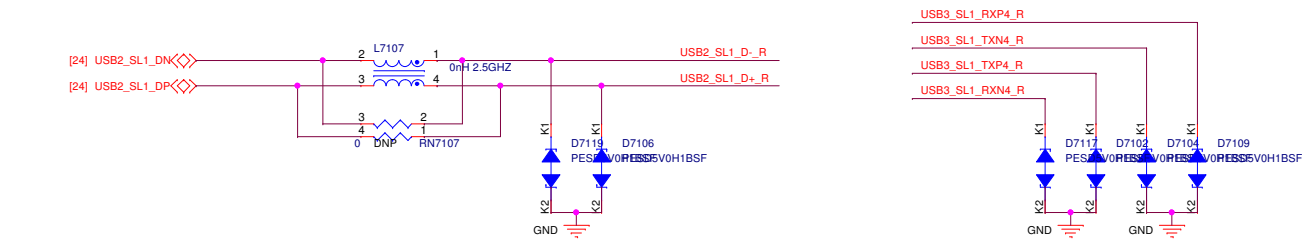
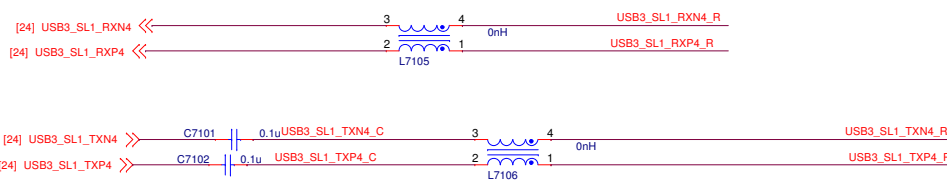
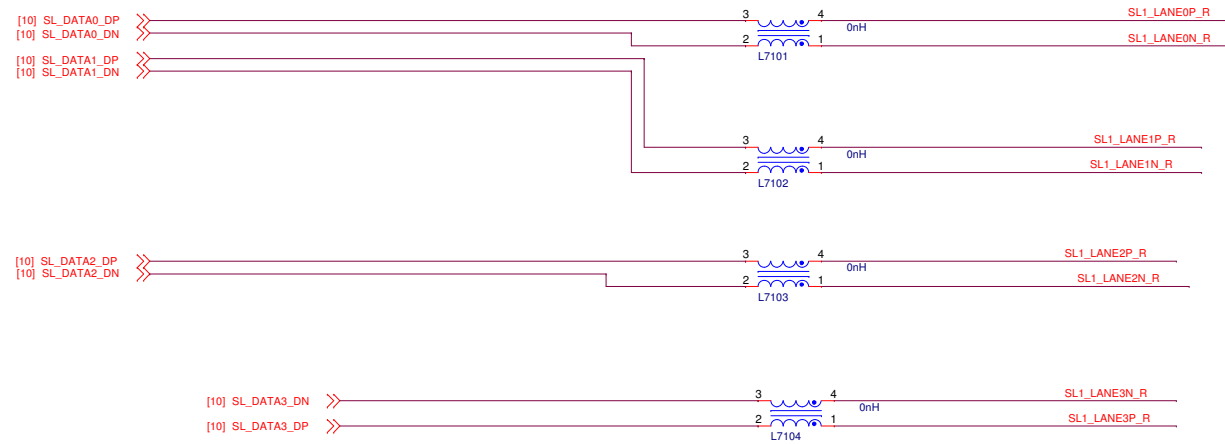
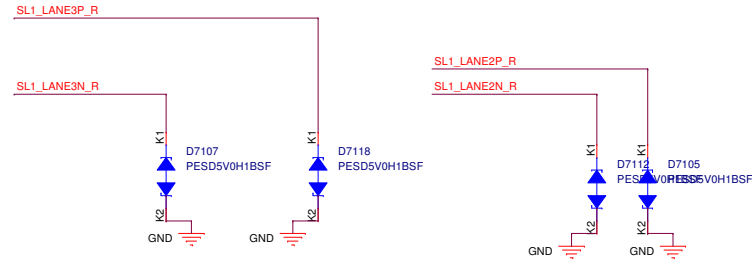


Switching Frequency (kHz)	Resistor to GND (Ω)		Mode	Resistor to GND (Ω)	Valley Current Limit (A)	Resistor to GND (Ω)
500	0		Non-interleaving, slew down	0	14	0
700	90k		Non-interleaving, decay	Float	20	90k
1000	150k		Interleaving, slew down	90k	26	150k
1200	Float		Interleaving, decay	150k	32	Float

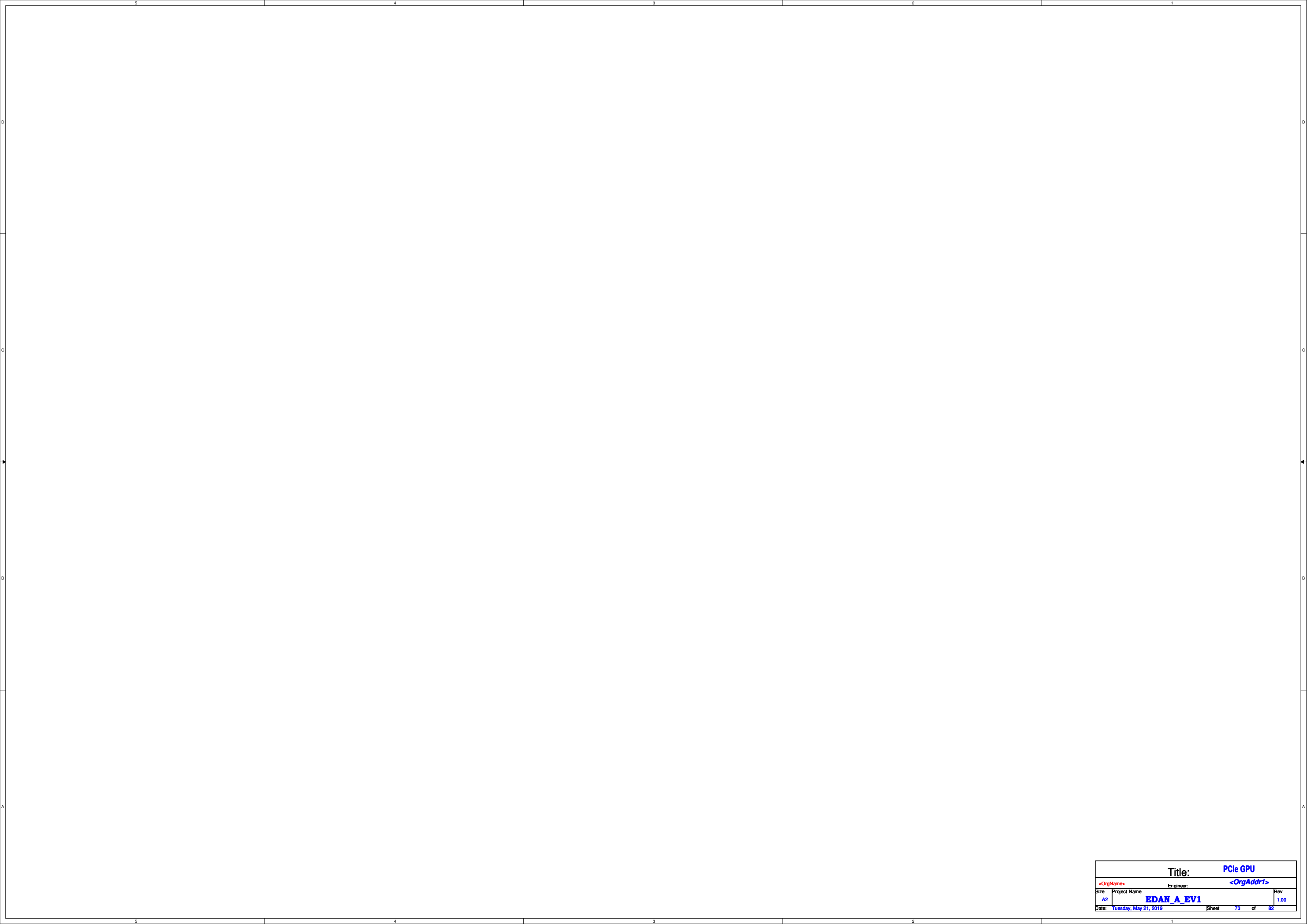
TRUTH TABLE		
S+ (PIN 8)	S- (PIN 10)	FUNCTION
X	0	D- = HSD1-
X	1	D- = HSD2-
0	X	D+ = HSD1+
1	X	D+ = HSD2+



Present State			Trigger	Output		
SL1_UART_TX	SL1_UART_RX	1W/2W Detect	Initial A/D read	SL1_UART_TX_SEL_N	SL1_UART_RX_SEL_N	SL Polarity
Low	Low	Detach	n/a	Low	Low	Detach
Low	High	1W	n/a	High	Low	Straight up
High	Low	1W	n/a	Low	High	Reversed
High	High	2W	Valid	Low	Low	Straight up
High	High	2W	Invalid	High	High	Reversed

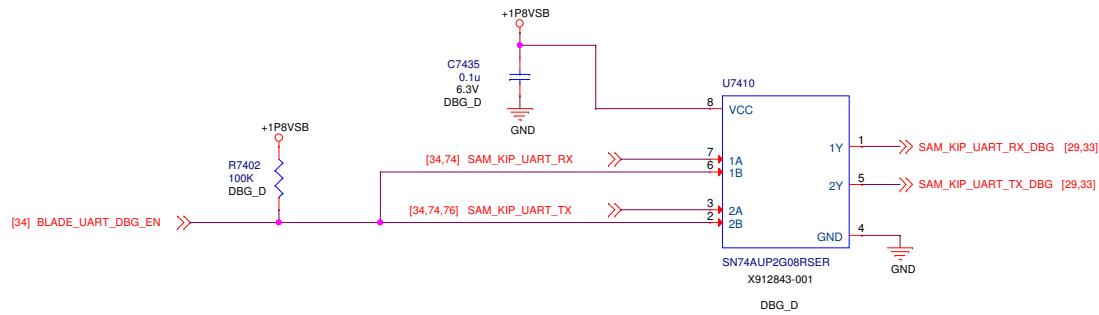
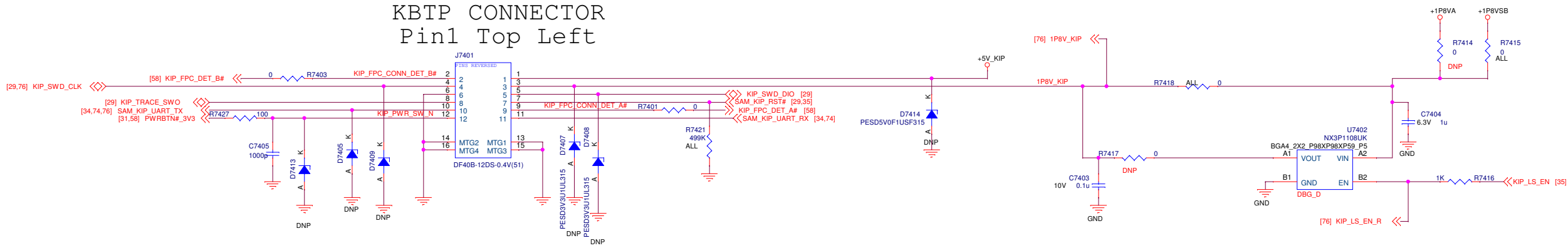


Title:		SL1 SIGNALS	
<OrgName>		<OrgAddr1>	
Engineer:			
Size	Project Name	Rev	
A2	EDAN_A_EV1	1.00	
Date:	Tuesday, May 21, 2019	Sheet	71 of 82



Title:		PCIe GPU	
<OrgName>		Engineer:	
Size	Project Name	Rev	
A2	EDAN_A_EV1	1.00	
Date:	Tuesday, May 21, 2019	Sheet	73 of 82

KBTP CONNECTOR
Pin1 Top Left

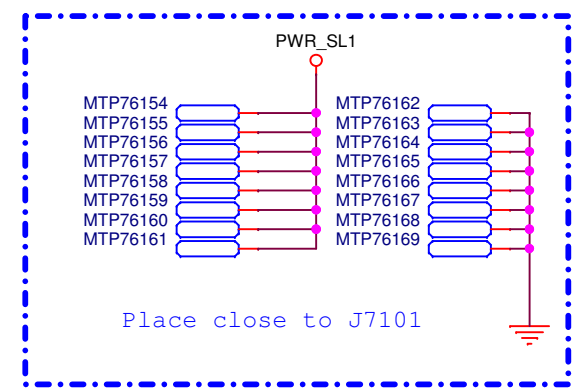
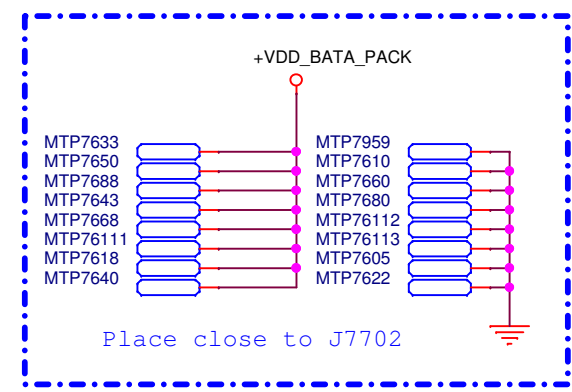
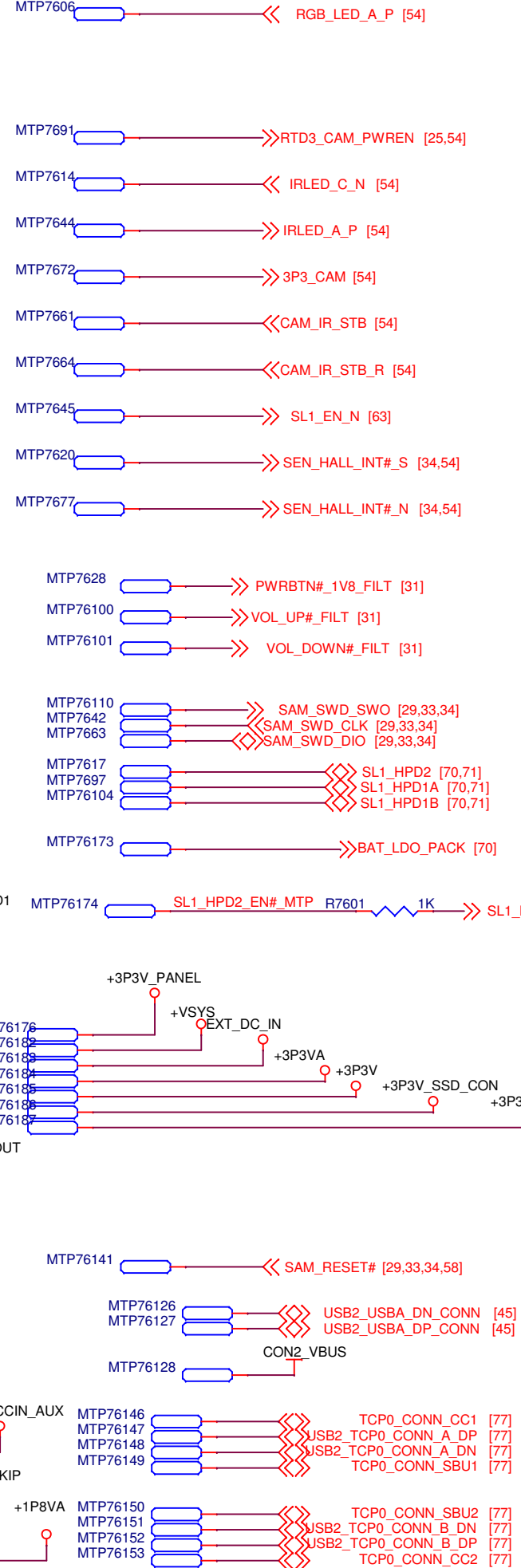
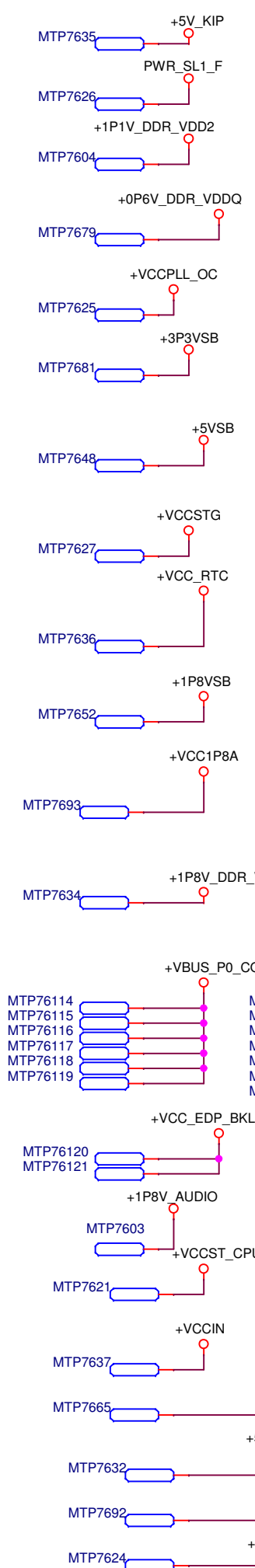
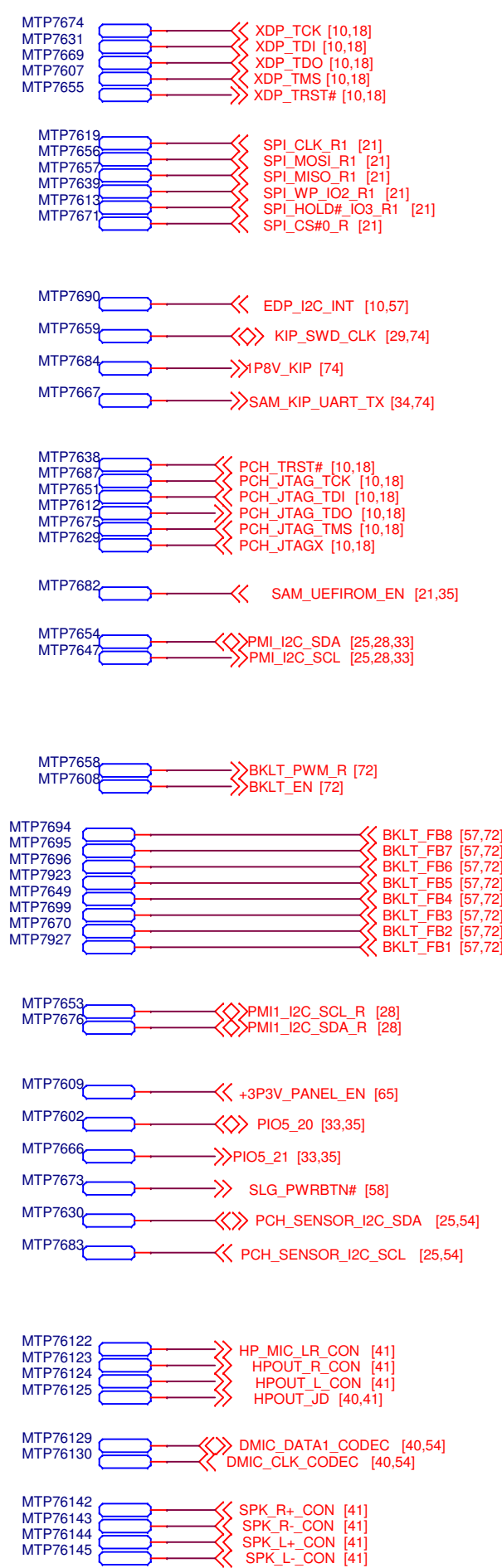


KIP UART Debug gated Sniffer (Dual AND gate,)
Place U7410 close to J7401 UART lines to minimize stubs

5	4	3	2	1
D				D
C				C
B				B
A				A

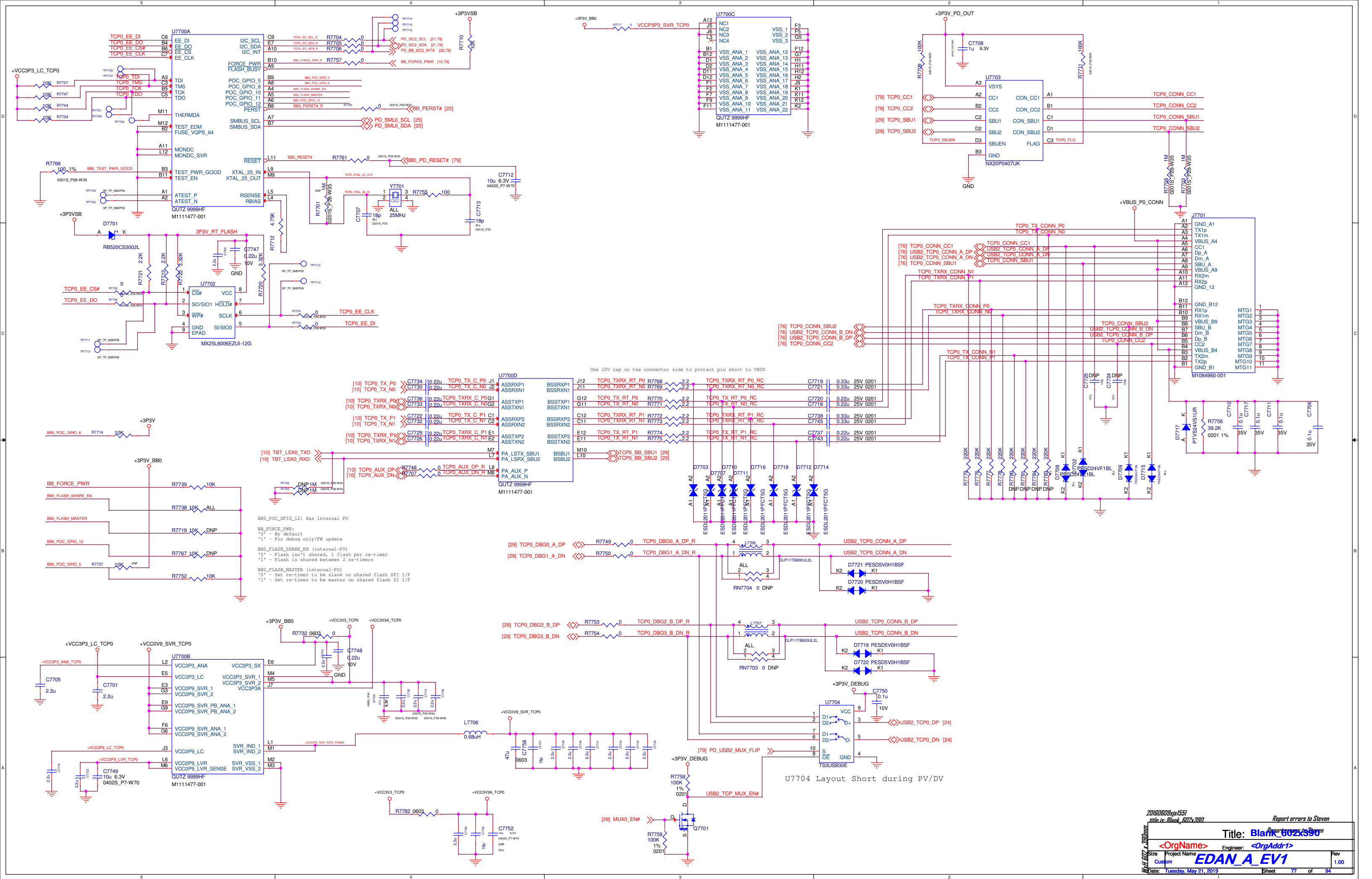
Title: Power Protect		
<OrgName> Engineer: <OrgAddr1>		
Size Custom	Project Name EDAN_A_EV1	Rev 1.00
Date: Tuesday, May 21, 2019	Sheet 75 of 82	

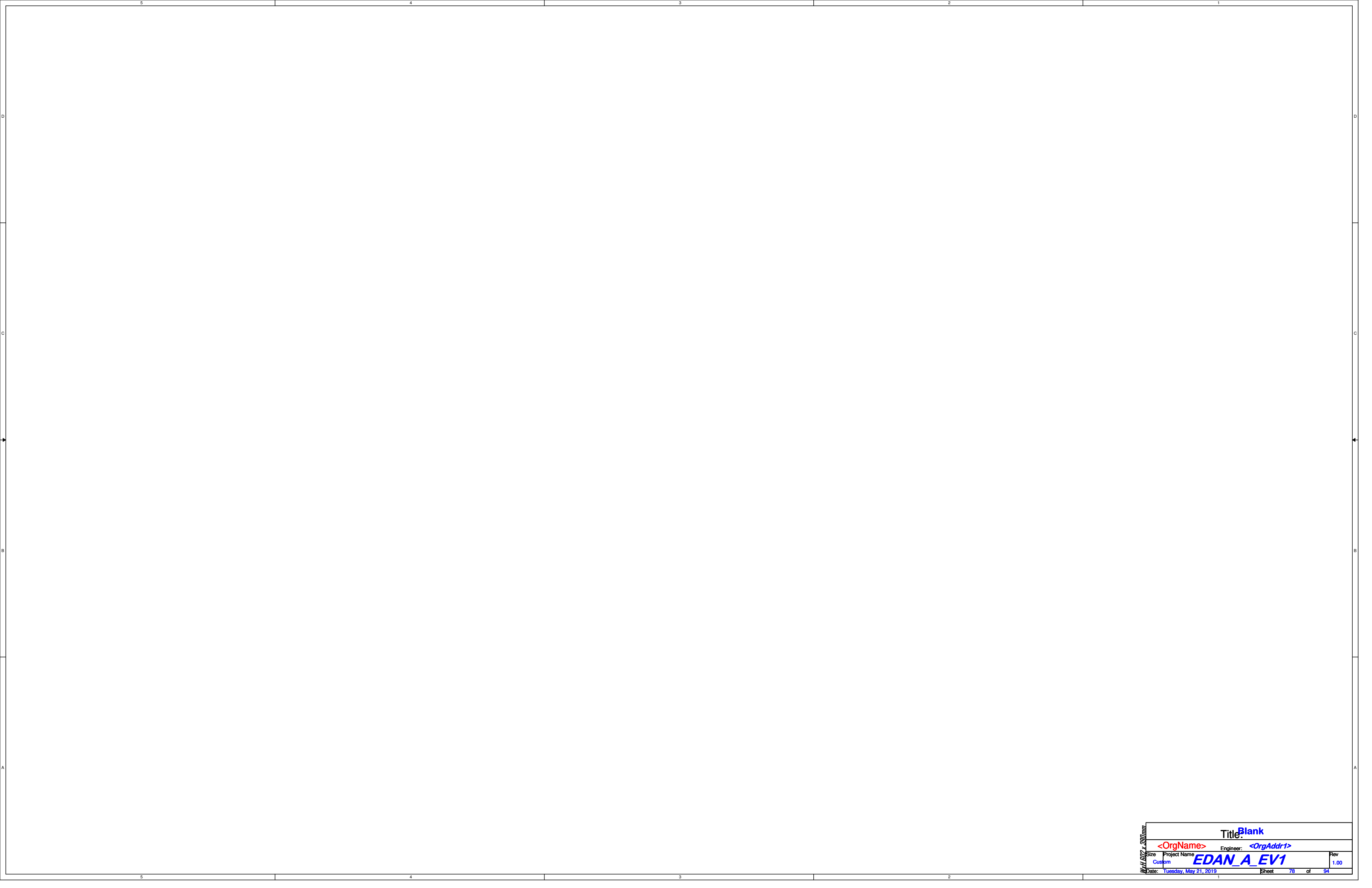
W x H 357 x 231 mm



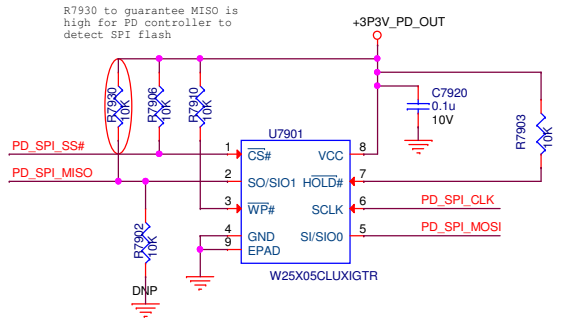
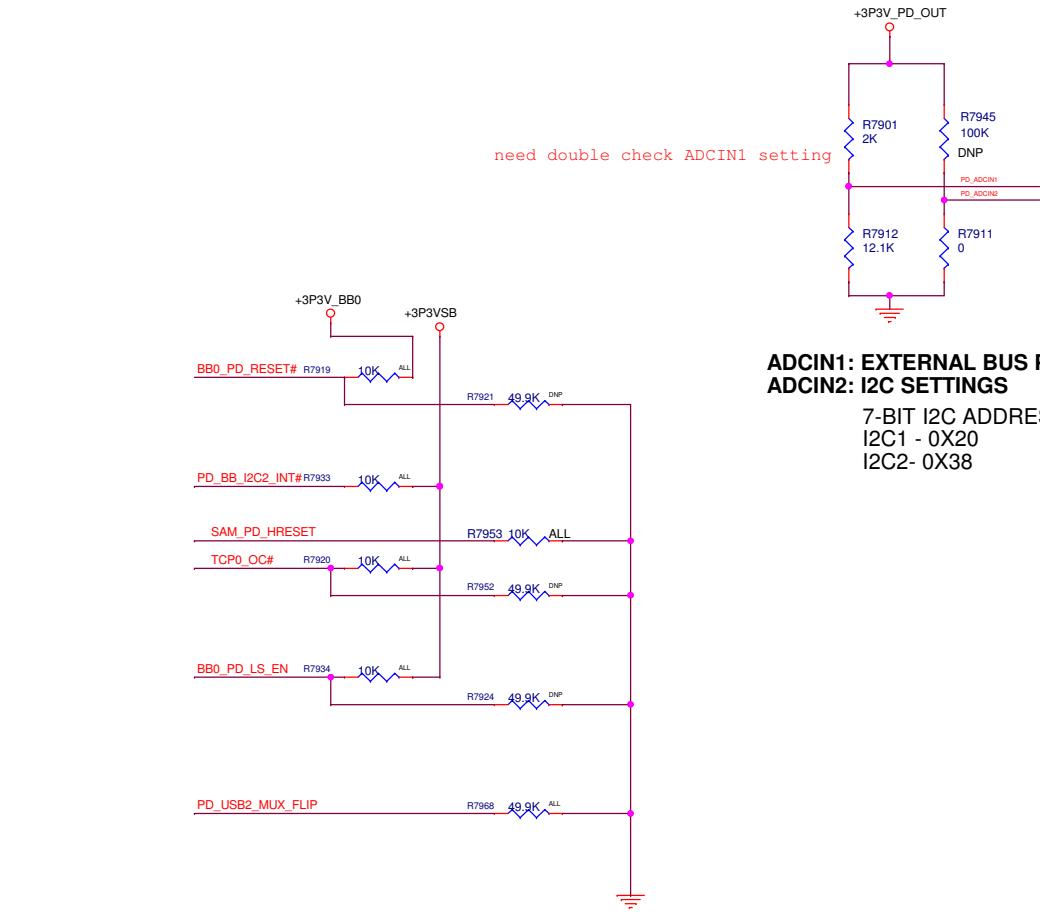
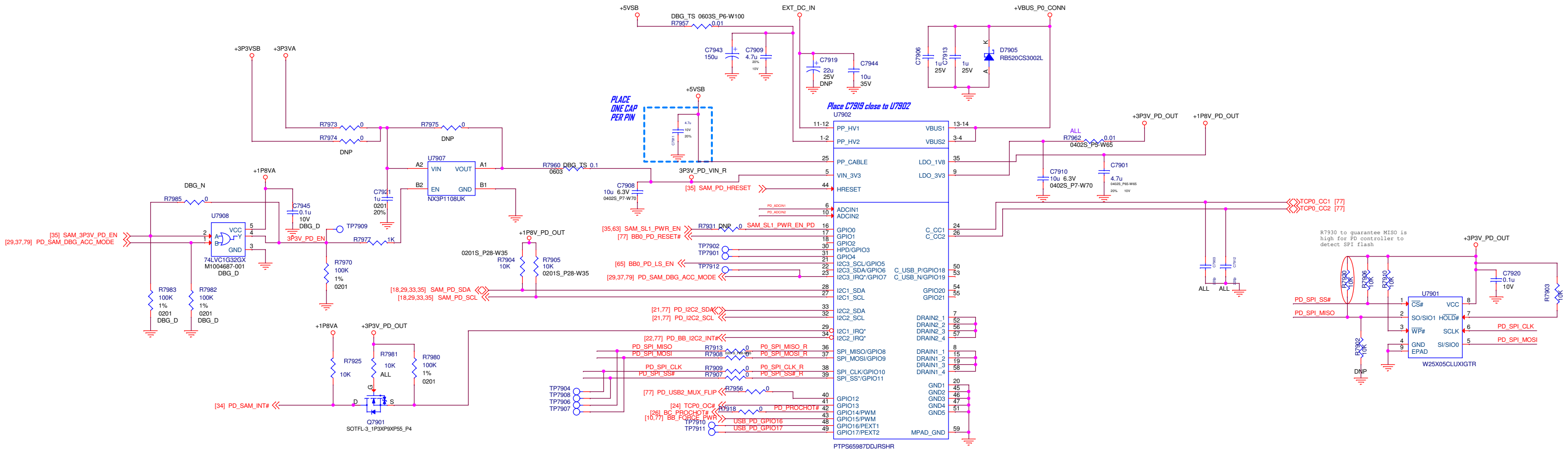
W x H 427 x 276 mm

Title: Frames, Holes, & Mechanical		
<OrgName>		Engineer: <OrgAddr1>
Size	Project Name	Rev
Custom	EDAN_A_EV1	1.00
Date: Tuesday, May 21, 2019	Sheet 76 of 82	

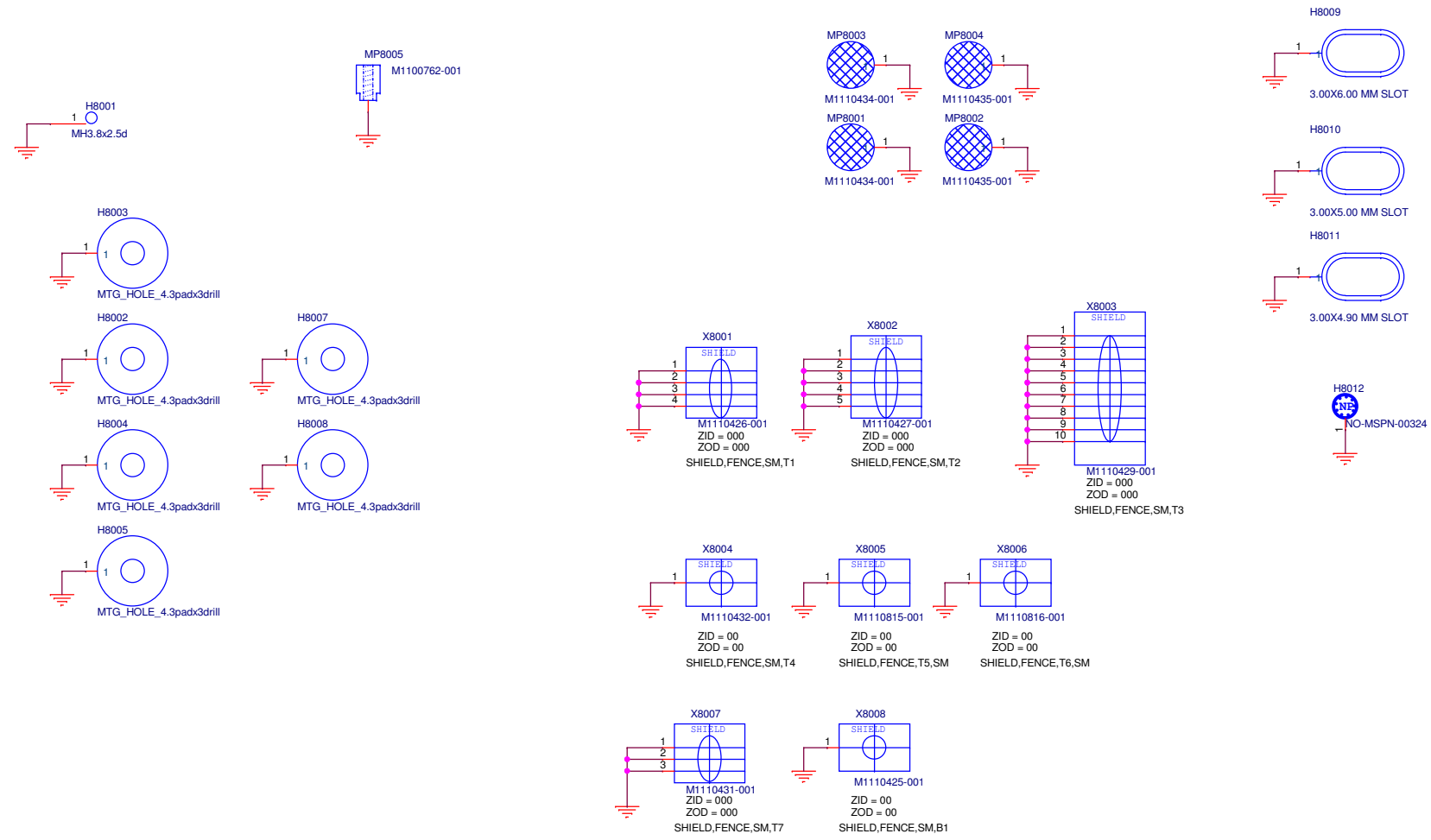


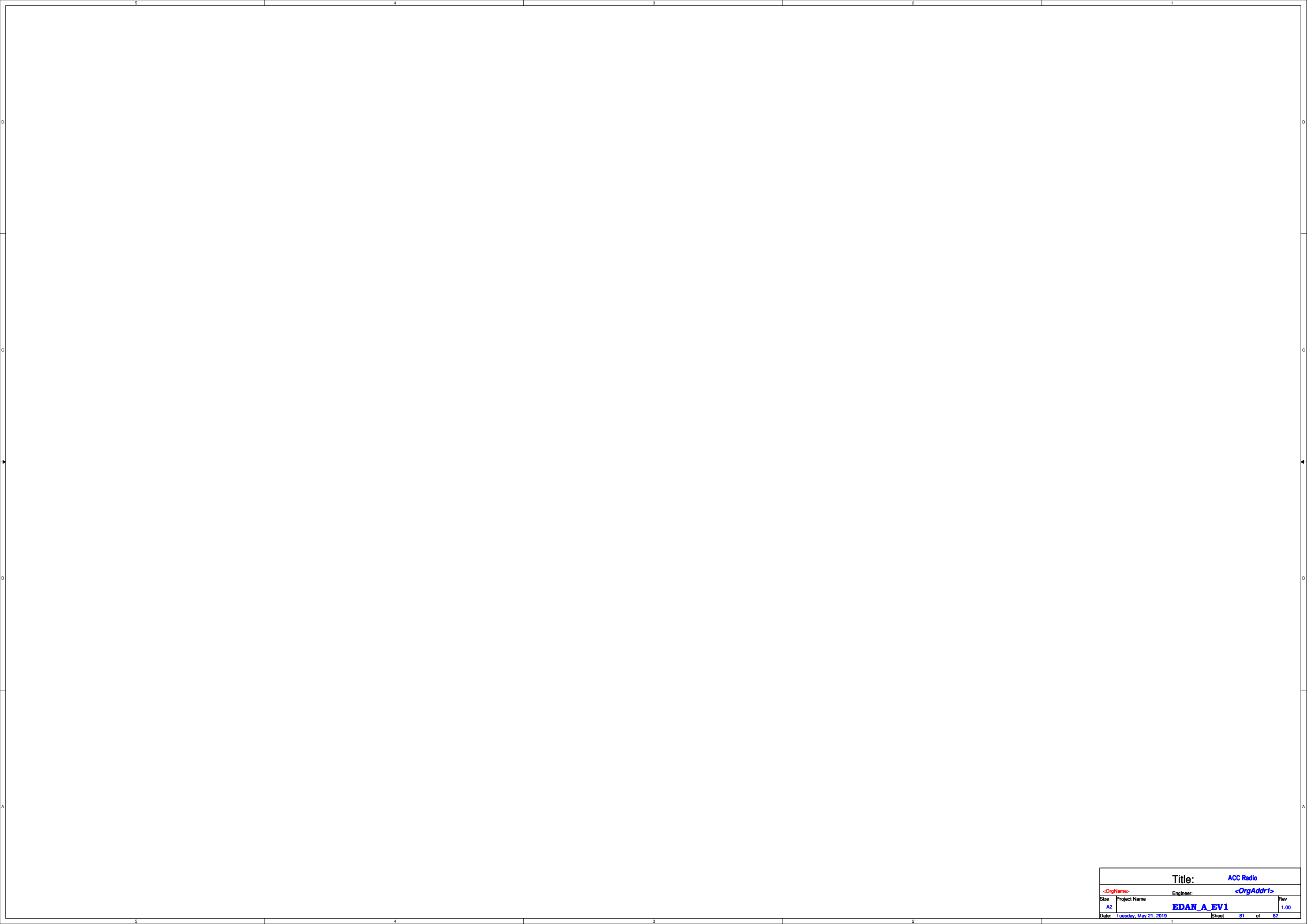


Title: Blank	
Engineer: <OrgAddr>	
Size: Custom	Project Name: EDAN_A_EV1
Date: Tuesday, May 21, 2019	Rev: 1.00
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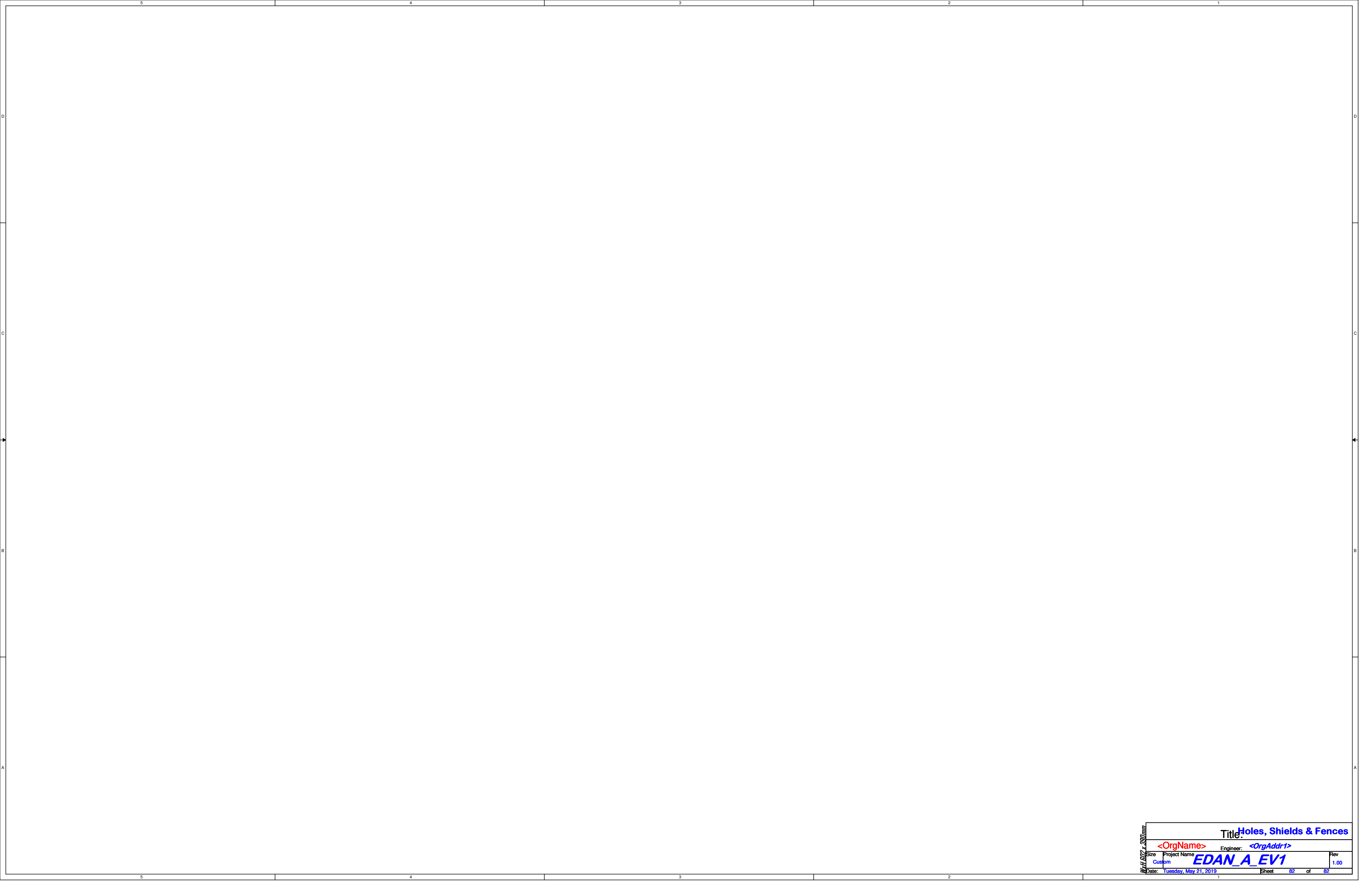


ADCIN1: EXTERNAL BUS POWER
ADCIN2: I2C SETTINGS
7-BIT I2C ADDRESS
I2C1 - 0X20
I2C2- 0X38





Title:		ACC Radio	
<OrgName>		Engineer: <OrgAddr1>	
Size	Project Name		Rev
A2	EDAN_A_EV1		1.00
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Title: Holes, Shields & Fences	
Engineer: <OrgAddr>	
Size: Custom	Project Name: EDAN_A_EV1
Date: Tuesday, May 21, 2019	Rev: 1.00
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Width 602 x 390mm